DC to 28GHz / 16dB / 23dBm Medium Power Amplifier

DATA SHEET **VWA 5000014 AA**

General Description

The **VWA5000014AA** is a distributed amplifier designed on a 0.15µm pHEMT process.

The device is capable of output voltage up to 8Vpp and has more than +23dBm of output power at saturation regime, up to 28GHz. It provides more than +21dBm of output power at 1dB of gain compression, up to 20GHz.The linear gain is of 16dB from DC to 28GHz, with an excellent group delay. The design has been optimized to provide high efficiency. The supply current is as low as 200mA when operating with V_D= +9V.

This device needs an RF Output external bias-tee to bias the drain and an RF Input external DC-Block.

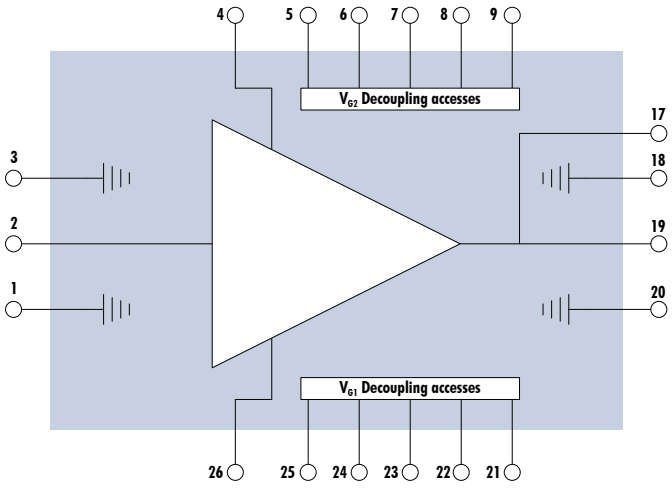
Features

- Distributed amplifier pHEMT GaAs MMIC
- Wide band : DC to 28GHz.
- Flat group delay (up to 32Gbps)
- 50ΩRF Single ended input and output
- DC coupled In, DC coupled Out
- P_{1dB} >+20dBm DC to 20GHz
- High output Psat >+21dBm DC to 28GHz
- Small signal gain >16dB typ. DC to 28GHz
- Power supply: 200mA @ +9V
- Chip size: 3.02 x 1.77 x 0.1 (mm)

Applications

- Wide Band Low Noise Amplifier
- Radar / ECM / ECCM
- Test and measurement
- E2O driver up to 32Gbps
- SONET / SDH.
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Symbol	Pad N°
RF In	2
V_{G2}	4
V_{G2} Decoupling access	5/6/7/8/9
V_{G1}	26
V_{G1} Decoupling access	21/22/23/24/25
RF Out & V_D	19
GND	1/2/18/20
V_{BIAS}	17

Electrical Specifications

Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D= +9V
- V_{G2}= +2V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		28	Ghz
NF	Simulated Noise figure		4.5		dB
G	Small signal gain		16		dB
ΔG	Small signal gain flatness		+/-1		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
P1dB	Output P1dB	20	21		dBm
P_{SAT}	Saturated output power		23		dBm
I_D	Drain current		200		mA

Environmental parameters

Symbol	Parameter	Values	Unit
Ta	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+85	°C

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_D	Drain bias voltage		9.5	V
V_{G2}	Gate control input access for second stage	-1	V_D/2	V
V_{G1}	Gate control input access for first stage	-1.5	0.15	V
Pin	RF input power		20	dBm
Pcw	Continuous power disspation		2	W
T process	Temperature process max 20 seconds		325	°C

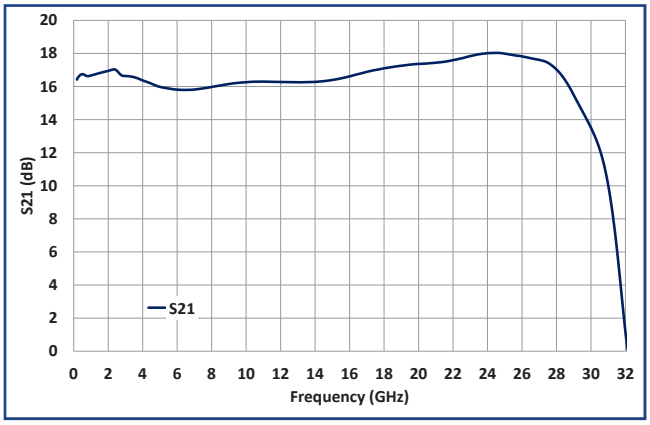
Operation of this device above any of these parameters may cause permanent damage.

Typical Performance (Test Under Probes)

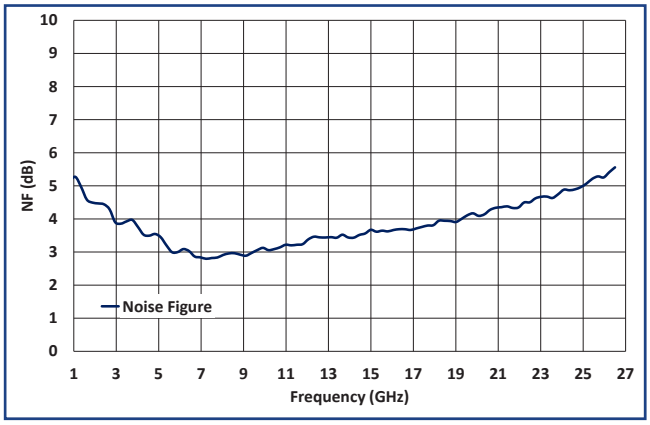
Measured assembly: see assembly diagram (except for RF Input and RF Output pads)

- Tamb.= +25°C
- V_D= +9V
- I_D= 200mA
- V_{G1}= 0V
- V_{G2}= +2V

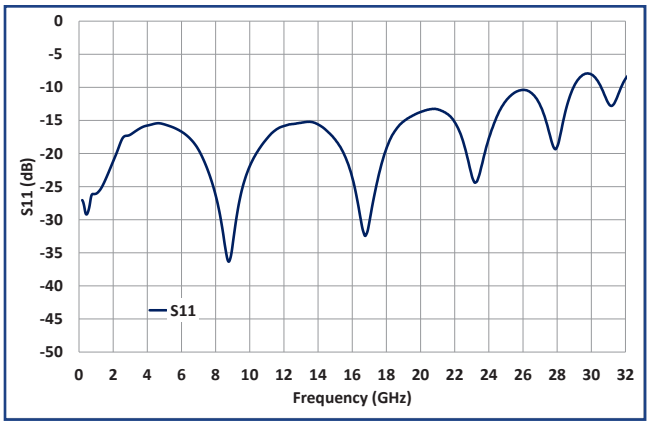
Small Signal Gain



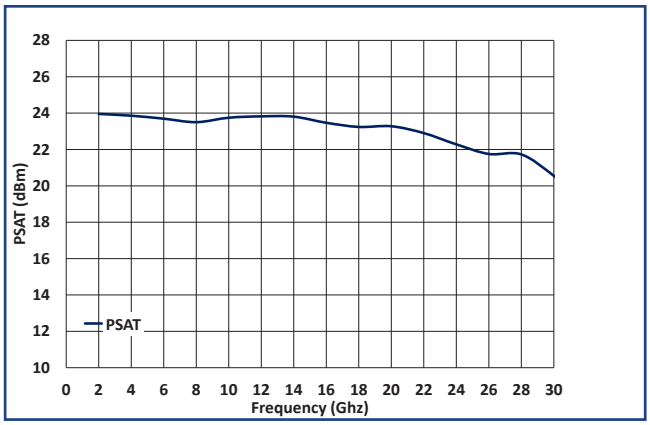
Noise Figure



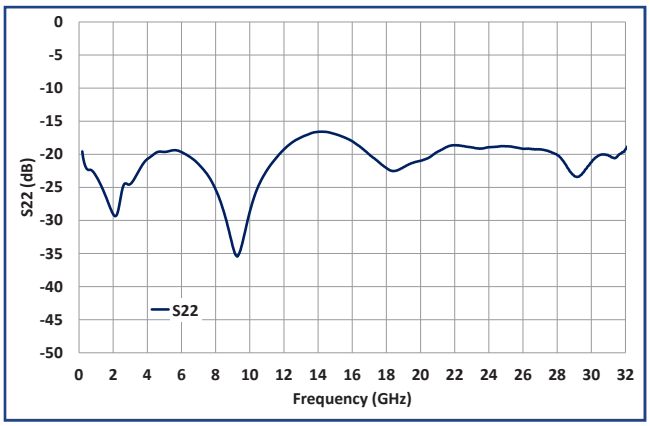
Input Return Loss



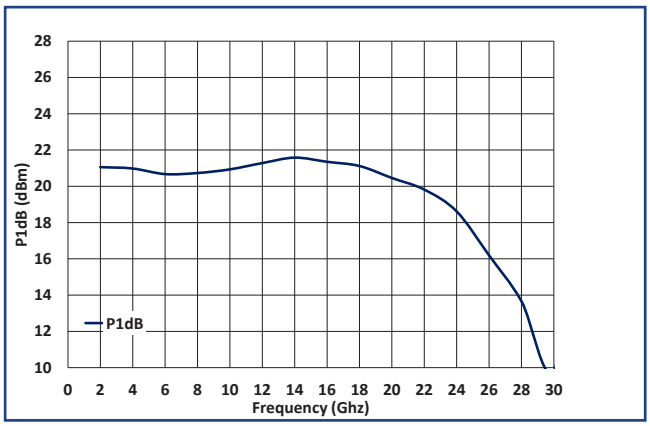
Saturated Output Power



Output Return Loss



Output P1dB

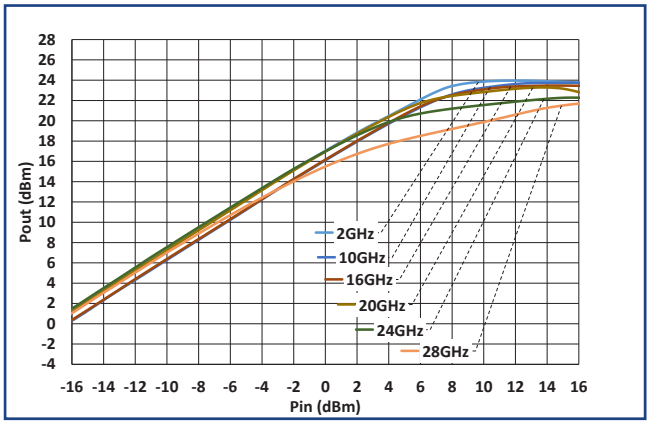


Typical Performance (Test Under Probes)

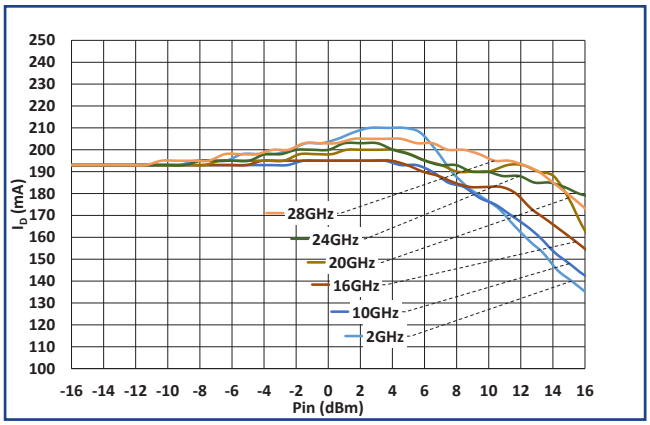
Measured assembly : see assembly diagram (except for RF Input and RF Output pads)

- Tamb.= +25°C
- V_D= +9V
- I_D= 200mA
- V_{G1}= 0V
- V_{G2}= +2V

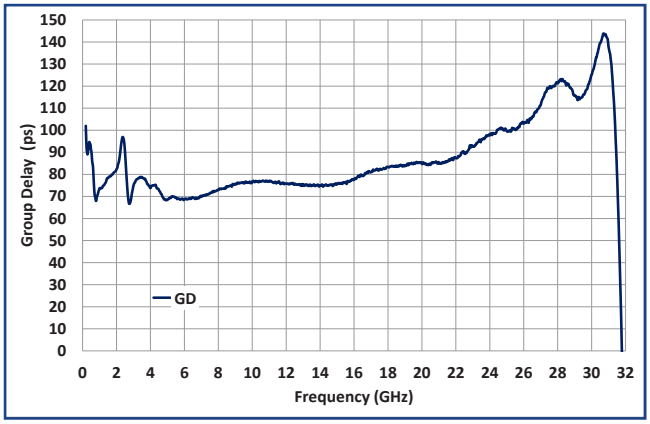
Output Power vs Input Power for various Frequency



Drain Current vs Input Power for various Frequency



roup Delay



Biasing procedure

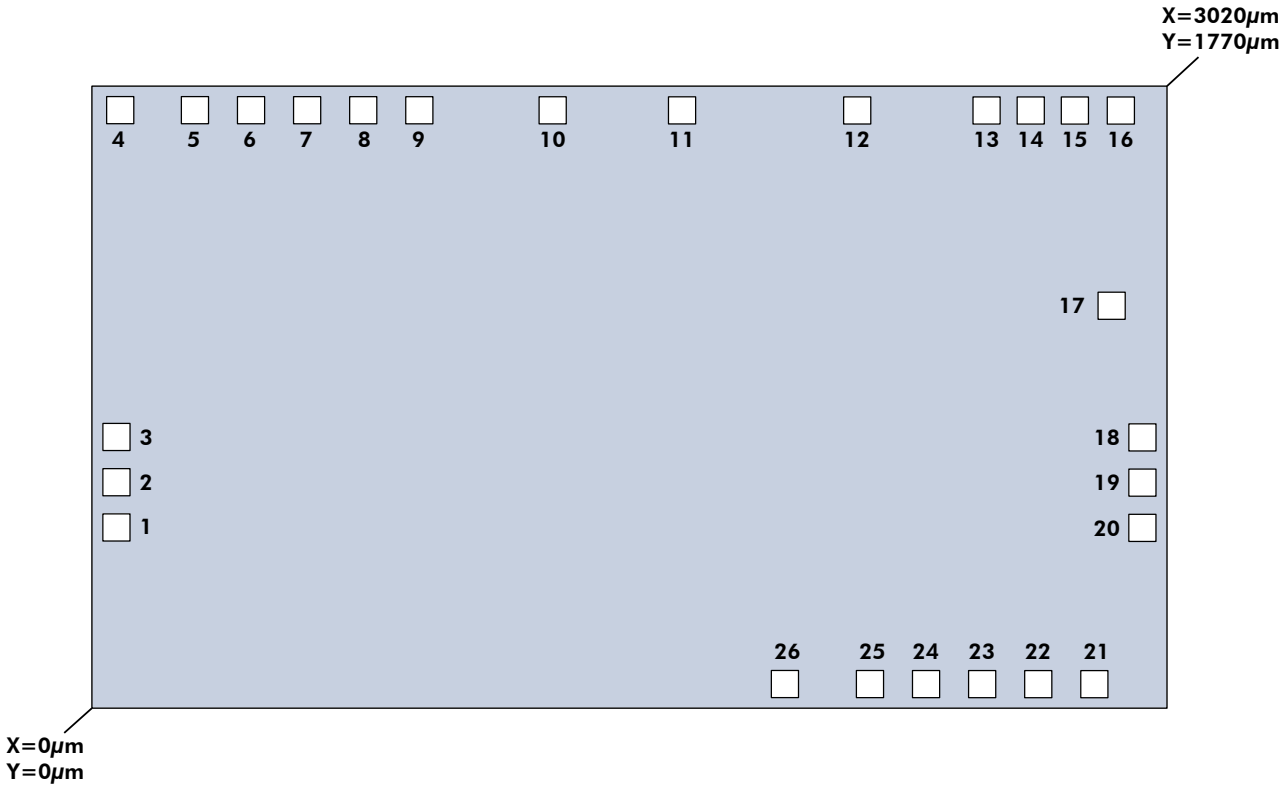
Switch on

1. Set V_D to +9V
2. Set V_{G2} to +2V
3. Turn RF Input ON

Switch off

1. Turn RF Input OFF
2. Decrease V_{G2} to 0V
3. Decrease V_D to 0V

Die Layout

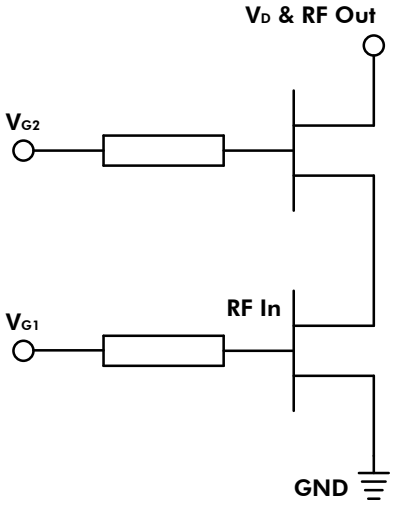
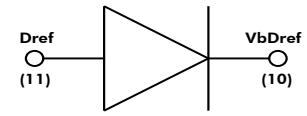
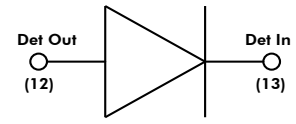
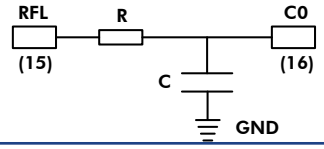


Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	90	533	75x75	GND
2	90	658	75x75	RF Input
3	90	784	75x75	V_{G2}
4	100	1686	75x75	GND
5	303	1686	75x75	D0
6	459	1686	75x75	D1
7	634	1686	75x75	D2
8	784	1686	75x75	D3
9	924	1686	75x75	D4
10	1240	1677	75x75	VbDref
11	1630	1677	75x75	Dref
12	2128	1677	75x75	Det Out
13	2485	1677	75x75	Det In
14	2607	1677	75x75	TC Out
15	2729	1677	75x75	RFL
16	2859	1677	75x75	C0
17	2816	1132	75x75	V_{BIAS}
18	2915	781	75x75	GND
19	2915	656	75x75	RF Output
20	2915	531	75x75	GND
21	2810	86	75x75	G0
22	2653	86	75x75	G1
23	2479	86	75x75	G2
24	2330	86	75x75	G3
25	2195	86	75x75	G4
26	1961	86	75x75	V_{G1}

Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

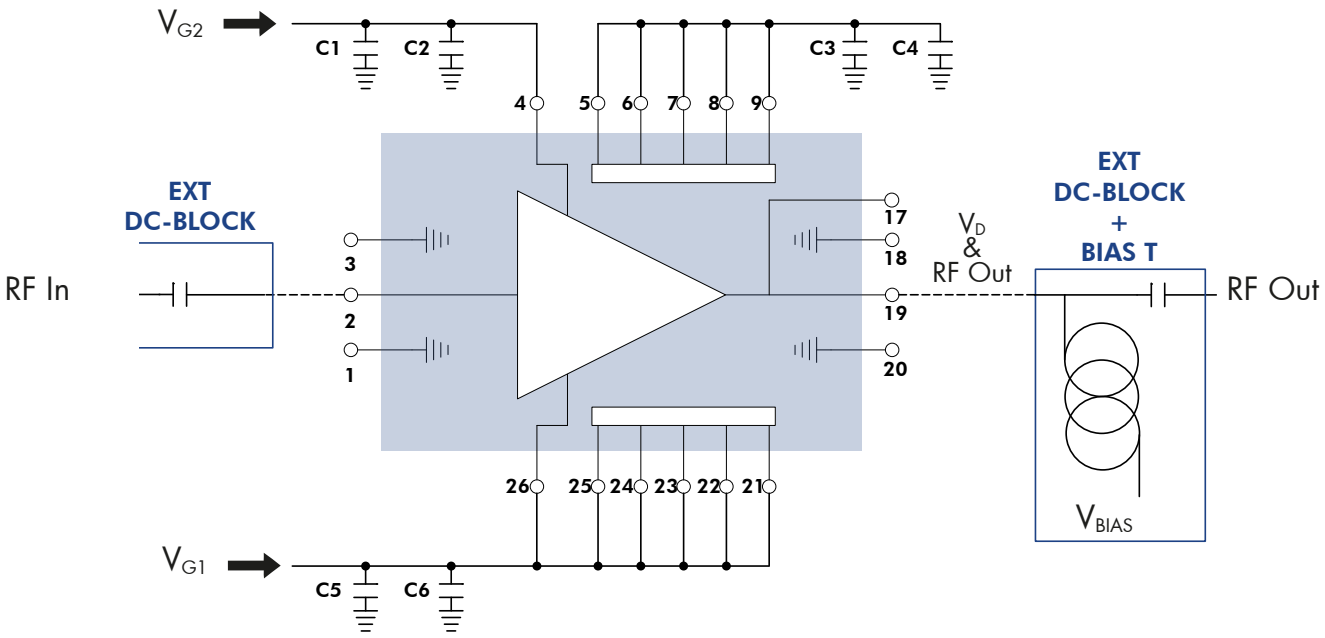
Access Description

Pin Number	Name	Description	Electrical interface
2	RF In	RF Amplifier input, this access is DC coupled and internally matched to 50Ω.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2.5V for nominal biasing conditions.	
5,6,7,8,9	D0 to D4	Decoupling accesses. These 5 accesses must be connected to a same MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire.	
17	V_{BIAS}	Pad linked to RF output. This pad can be connected to the RF OUT 50Ω transmission line (additionally to the RF Output pad wiring)	
19	RF Out	RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to bias the drain current (I_D), by using a wide bandwidth external Bias-T structure.	
26	V_{G1}	Gate control input access for first stage distributed amplifier structure. Must be connected to a MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire. It can also be directly connected to the ground reference plane.	
10	VbDref	Reference diode polarization (*)	
11	Dref	Reference diode output (*)	
12	DetOut	Detector output (*)	
13	Det In	Detector input (*)	
14	TC Out	Coupler output, connect to Det I (Pin 13) to use as a detector (*)	
15	RFL	Embedded serial 55Ω serial resistor	
16	C0	Embedded parallel 1pF capacitor	
21, 22, 23 24, 25	G0 to G4	V_{G1} decoupling accesses. This 5 accesses must be connected to V_{G1}	
Die Bottom	GND	Die must be connected to RF and DC Ground	

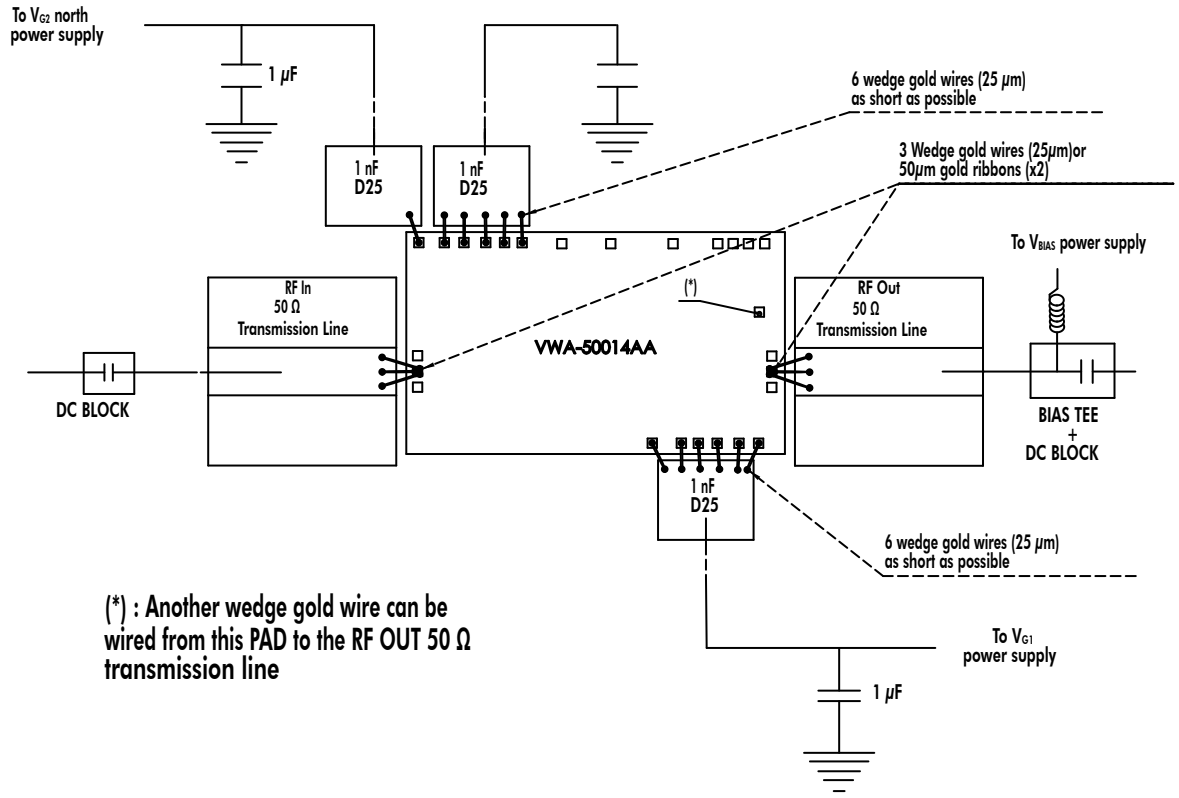
(*) See application note VWA_50014_AAAB_AN_ Ed1.0.)

Application Circuit

- C1, C4 and C5: 1µF
- C2, C3 and C6: 1nF capcitors are MIM type and must be placed as close as possible to the die access.



Typical Assembly Diagram



Ordering Information

Product Code	Definition
VWA 5000014 AA	DC to 28GHz / 16dB / 23dBm

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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