DC to 27GHz / 13dB / 18dBm Low Noise Amplifier

DATA SHEET **VWA 5000015 AB**

General Description

The **VWA5000015AB** is a wide band distributed amplifier designed on a 150nm pHEMT process that operates up to 31GHz, with flat group delay.

The device is capable of more than 19 dBm saturated output power, and provides more than 13dB of gain from DC to 27GHz with less than 1dB of flatness. It integrates an output power detector for monitoring function. A 24dB tap coupler delivers the image of the output level on a dedicated pad, and a peak detector is available on the die. Connecting the input of the peak detector to the tap coupler output will generate a DC signal for monitoring the output signal level in the RF spectrum. A reference diode is also available for temperature reference information of the detector function.

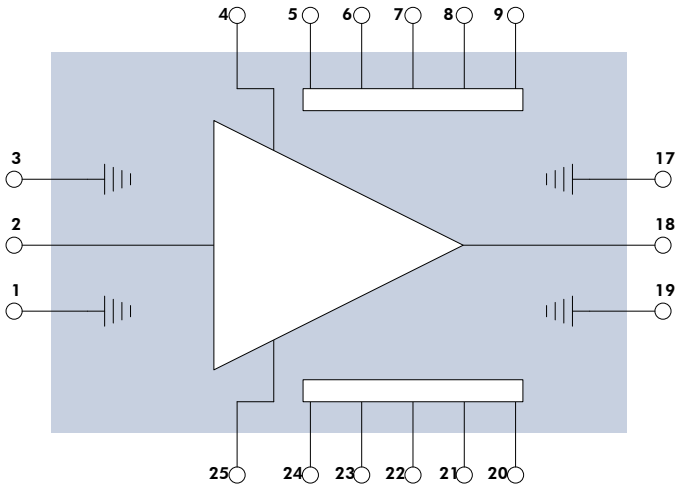
Features

- Distributed amplifier pHEMT GaAs MMIC.
- Frequency Range:
  - DC to 27GHz @ 1dB flatness.
  - DC to 31GHz @ 3dB cut_off.
- Bessel response up to 40GHz with flat group delay.
- 50Ω Single ended RF input and output, DC coupled.
- Integrated output power tap coupler.
- Integrated output level detection.
- Reference diode output.
- OP1dB Up to 15dBm (DC to 27GHz)
- P_{SAT} Up to 18dBm
- Small signal gain : 13dB from DC to 27GHz
- Power supply: 125mA @ +8V
- Chip size: 2.97 x 1.52 x 0.10 (mm)

Applications

- Wide Band Low Noise Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Broadband radio communication
- Optical communication: NRZ 10, 28 to 32GBps
- NRZ Nyquist Filtered 56GBps

Pins Assignement & Functional Block Diagram



Symbol	Pad N°
RF In	2
V_{G2}	4
V_{G2} Coupling	5/6/7/8/9
V_{G1}	25
V_{G1} Coupling	20/21/22/23/24
RF Out & V_D	18
GND	1/3/17/19

Electrical Specifications (Test Under Probes)

Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D= +8V
- V_{G1}= 0V
- V_{G2}= +2V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		27	Ghz
NF	Noise figure		3.5	5	dB
G	Small signal gain		13		dB
ΔG	Small signal gain flatness		+/-0.5		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
Bw@3dB	Frequency Bandwidth @3dB		31		GHz
P1dB	Output P1dB		16.5		dBm
P_{SAT}	Saturated output power		19		dBm
TC	Output tap coupler ratio		24		dB
ΔGD	Group delay variation		+/-10		ps
I_D	Drain current		125		mA

Environmental parameters

Symbol	Parameter	Values	Unit
Top	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+85	°C

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_D	Drain bias voltage		9	V
V_{G2}	Gate control input access for second stage		V_D/2	V
V_{G1}	Gate control input access for first stage	-1.5	+0.15	V
Pin	RF input power		+20	dBm
Pcw	Continuous power disspation		1.35	W
T process	Temperature process max 20 seconds		325	°C

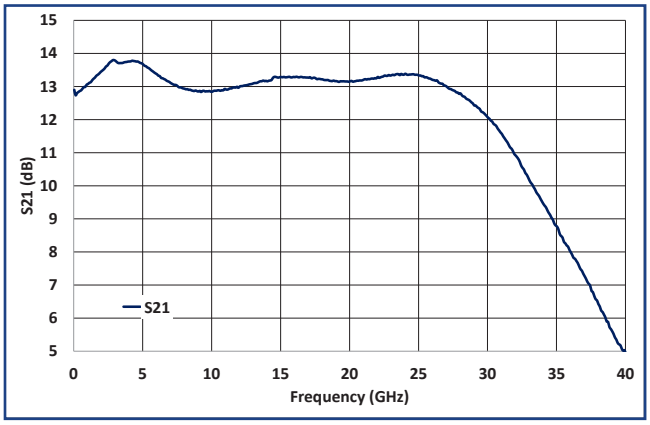
Operation of this device above any of these parameters may cause permanent damage.
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Typical Performances (Test Under Probes)

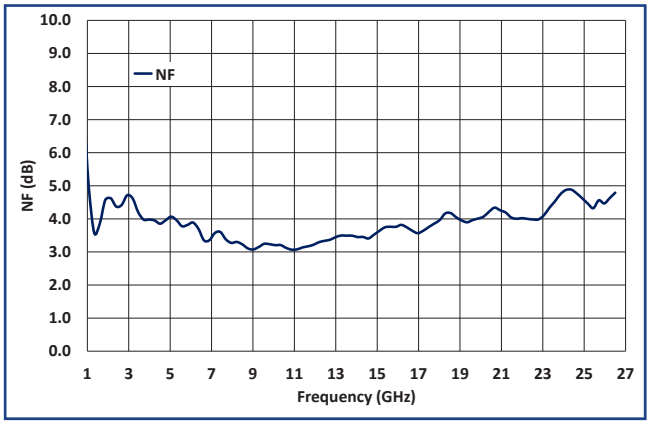
Measured assembly: see assembly diagram (except for RF Input and RF Output pads)
Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D= +8V
- I_D= 125mA
- V_{G1}= 0V
- V_{G2}= +2V

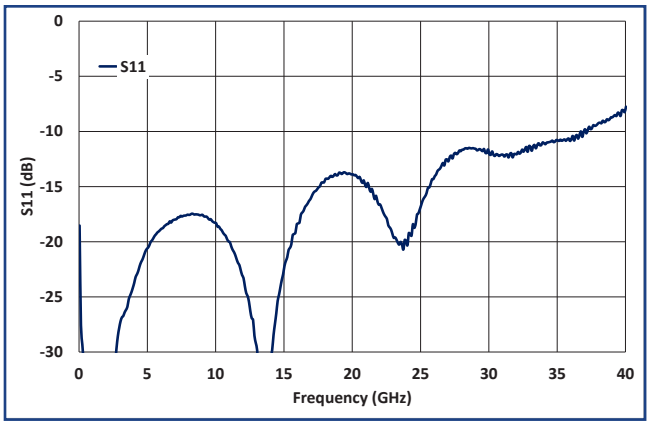
Small Signal Gain



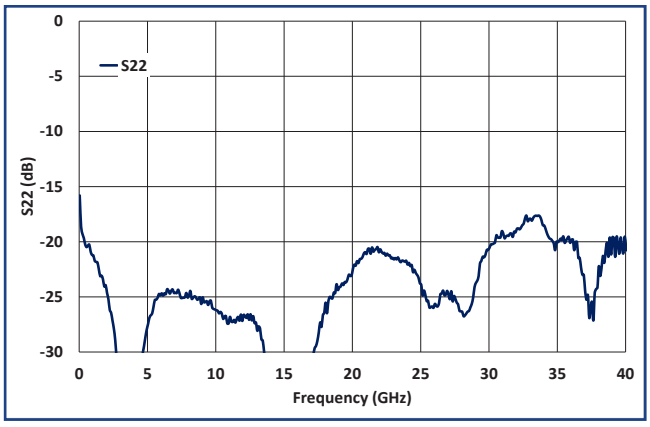
Noise Figure



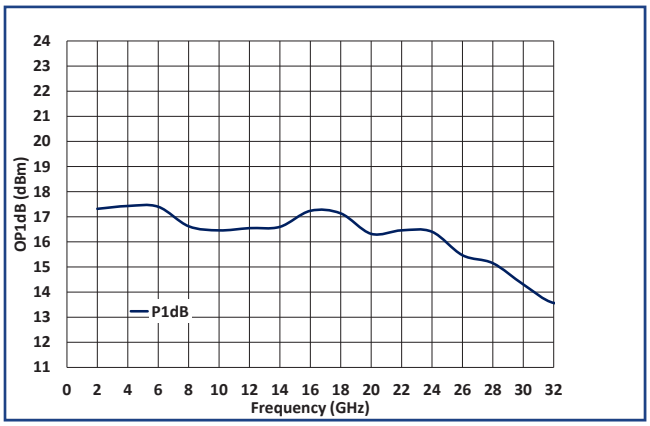
Input Return Loss



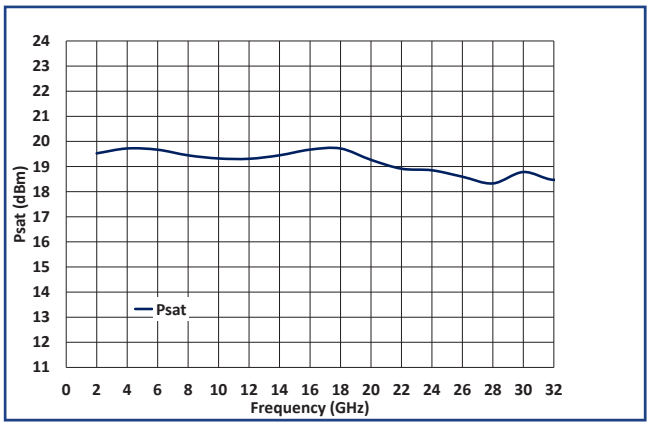
Output Return Loss



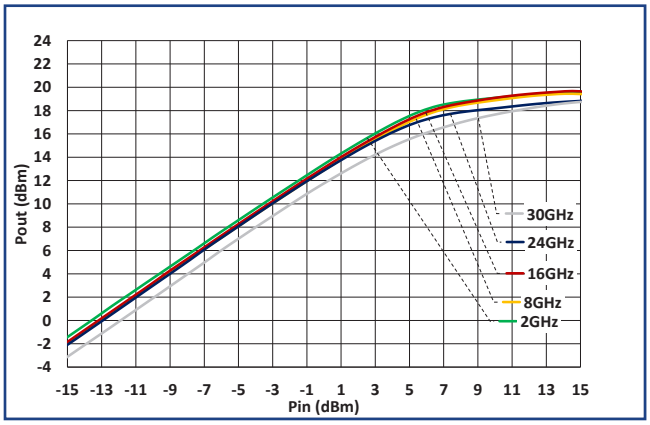
Output P1dB



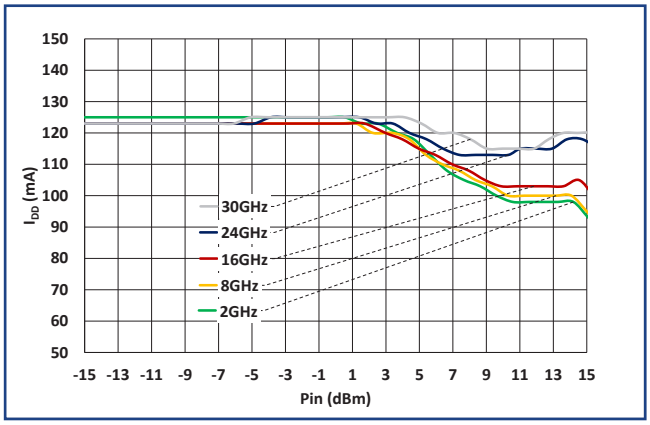
Saturated Output Power



Output Power VS Input Power for various Frequency



Drain Current VS Input Power for various Frequency



Biasing procedure

Switch on

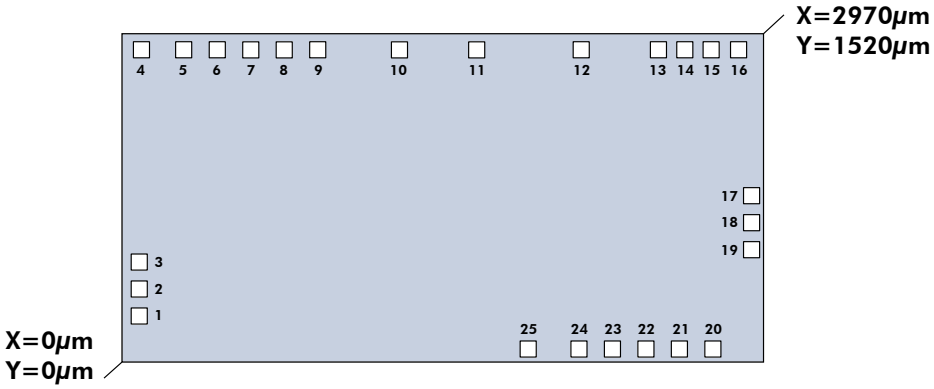
1. Set V_{G1} to 0V
2. Set V_D to +8V
3. Set V_{G2} to +2V
4. Adjust V_{G1} to obtain the specified Drain current ID
4. Turn RF Input ON

Note : V_{G1} can be directly connected to the ground, for some application

Switch off

1. Turn RF Input OFF
2. Set V_{G2} to 0V
3. Set V_D to 0V
2. Set V_{G1} to 0V

Die Layout

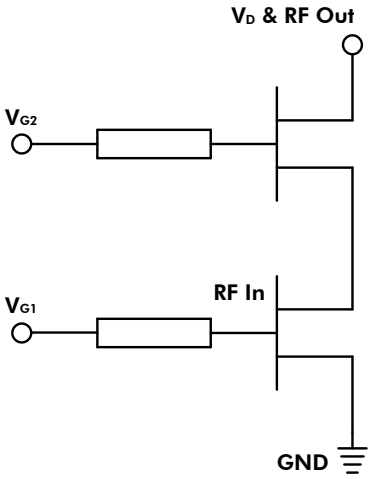
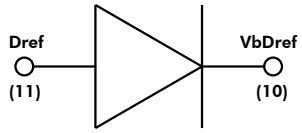
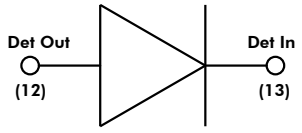
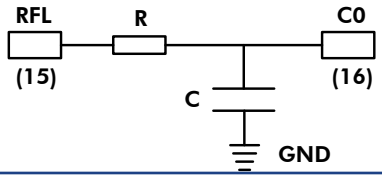


Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	67	220	75x75	GND
2	67	345	75x75	RF Input
3	67	470	75x75	V_{G2}
4	77	1452	75x75	GND
5	273	1452	75x75	D0
6	428	1452	75x75	D1
7	583	1452	75x75	D2
8	738	1452	75x75	D3
9	893	1452	75x75	D4
10	1272	1452	75x75	VbDref
11	1629	1452	75x75	Dref
12	2113	1452	75x75	Det Out
13	2471	1452	75x75	Det In
14	2593	1452	75x75	TC Out
15	2715	1452	75x75	RFL
16	2842	1452	75x75	C0
17	2902	777	75x75	GND
18	2902	652	75x75	RF Out & V_D
19	2902	527	75x75	GND
20	2723	67	75x75	G0
21	2568	67	75x75	G1
22	2413	67	75x75	G2
23	2258	67	75x75	G3
24	2103	67	75x75	G4
25	1868	67	75x75	V_{G1}

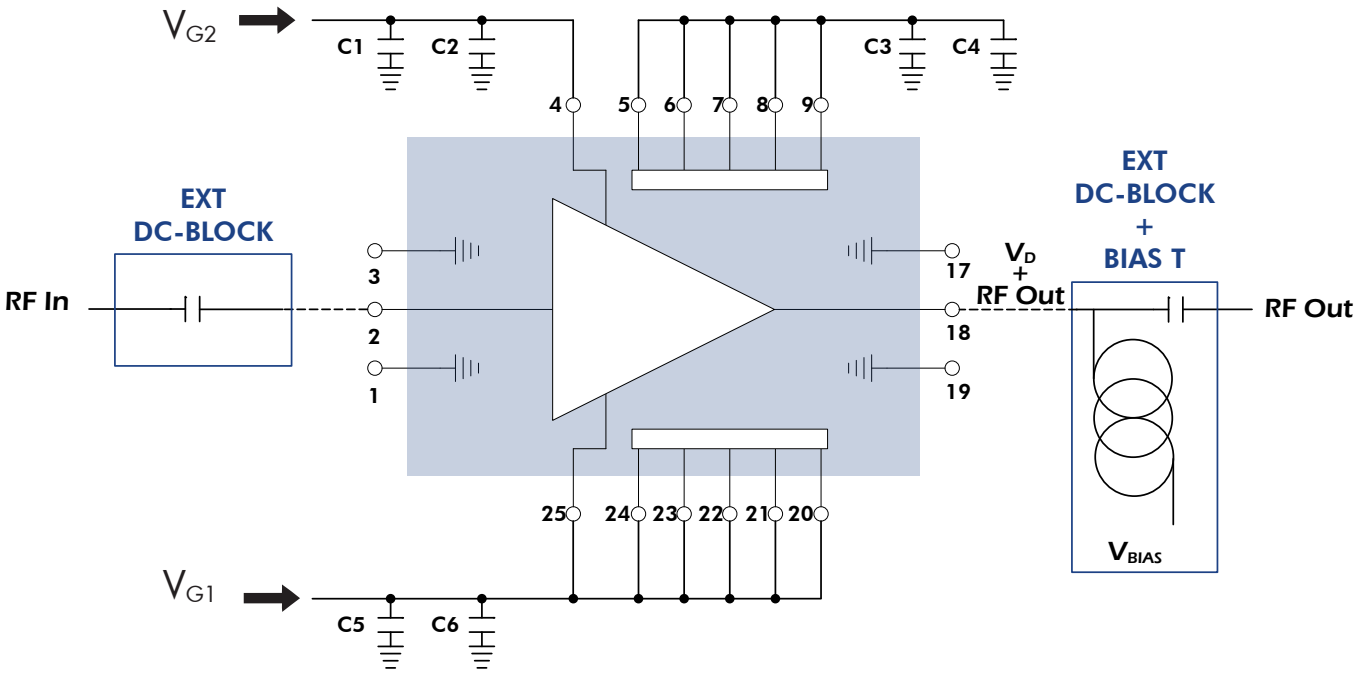
Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

Access Description

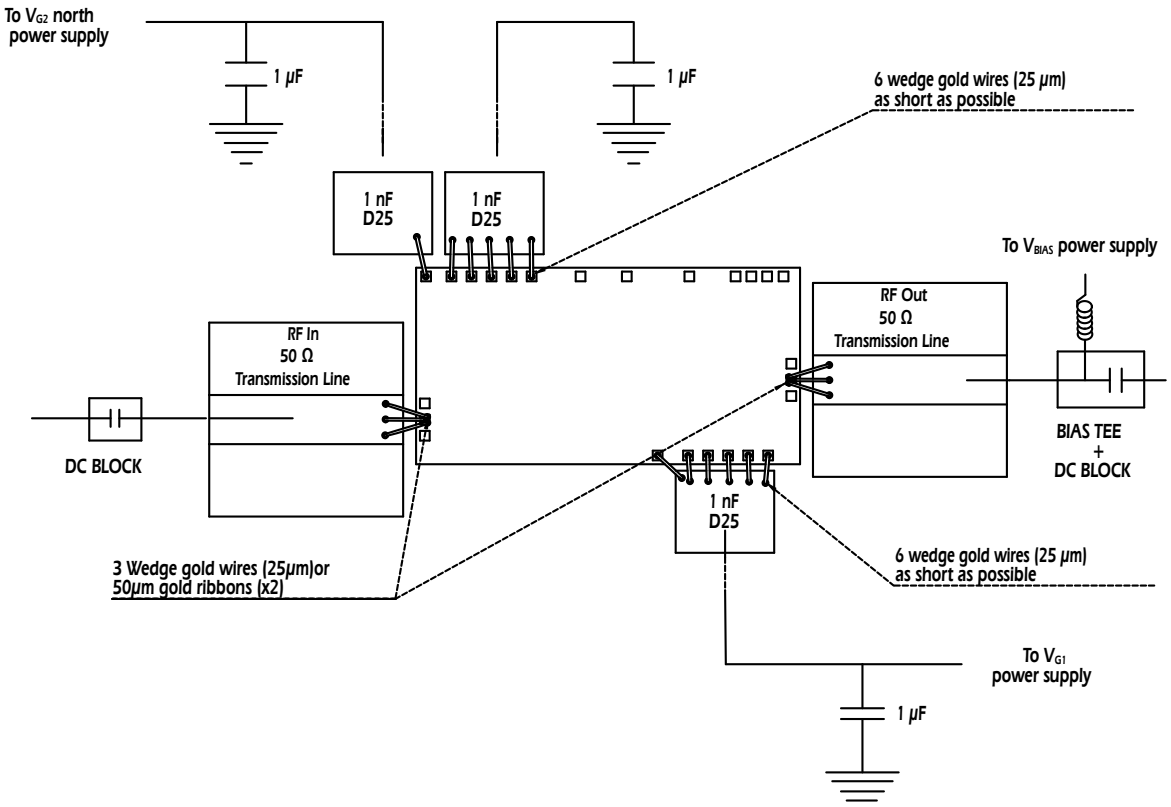
Pin Number	Name	Description	Electrical interface
2	RF Input	RF Amplifier input, this access is DC coupled and internally matched to 50Ω.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2V for nominal biasing conditions.	
5,6,7,8,9	D0 to D4	Decoupling accesses. These 5 accesses must be connected to a same MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire.	
18	RF Output	RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to bias the drain current (I_D), by using a wide bandwidth external Bias-T structure.	
20,21,22, 23,24	G0 to G4	V_{G1} decoupling accesses. These 5 accesses must be connected to V_{G1}	
25	V_{G1}	Gate control input access for first stage distributed amplifier structure. Must be connected to a MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire. It can also be directly connected to the ground reference plane.	
10	VbDref	Reference diode polarization	
11	Dref	Reference diode output	
12	DetOut	Detector output	
13	Det In	Detector input	
14	TC Out	Coupler output, connect to Det I (Pin 13) to use as a detector	
15	RFL	Embedded serial 55Ω serial resistor	
16	C0	Embedded parallel 1pF capacitor	
Die Bottom	GND	Die must be connected to RF and DC Ground	

Application Circuit

- C1, C4 and C5 = 1µF
- C2, C3 and C6 1µF capcitors are MIM type and must be placer as close as possible to the die access.



Typical Assembly Diagram



Ordering Information

Product Code	Definition
VWA 5000015AB	DC To 27GHz - 13dB - 18dBm

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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