

## General Description

The **VWA500025AA** is a distributed amplifier designed on a 0.15µm pHEMT process.

The device is capable of more than +16dBm of output power at saturation regime, up to 40GHz. It provides more than +14dBm of output power at 1 dB of gain compression, up to 40GHz. The linear gain is of 11dB from DC to 40GHz, with an excellent group delay. The design has been optimized to provide high efficiency. The supply current is as low as 100mA when operating with V<sub>D</sub>= +8V.

This device needs a RF output external bias-tee to bias the drain and a RF input external DC-Block.

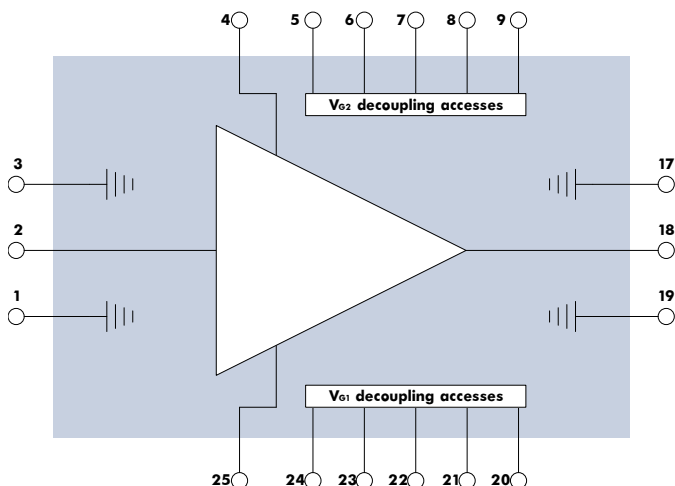
## Features

- Wideband distributed amplifier pHEMT GaAs MMIC
- Wide band: DC to 45GHz.
- Flat group delay (up to 64Gbps)
- 50ΩRF Single ended input and output
- DC coupled In, DC coupled Out
- P<sub>1dB</sub>: +14dBm DC to 40GHz
- P<sub>SAT</sub> >+16dBm DC to 40GHz
- Small signal gain: >10dB from DC to 45GHz
- Power supply: 100mA @ +8V
- Chip size: 3.02 x 1.57 x 0.1 (mm)

## Applications

- Wide Band Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Fiber transmission NRZ, PAM4 : 56 / 64 GBPS
- Broadband / datalink communication

## Pins Assignment & Functional Block Diagram



Symbol	Pad N°
RF In	2
V <sub>G2</sub>	4
V <sub>G2</sub> decoupling accesses	5/6/7/8/9
V <sub>G1</sub>	25
V <sub>G1</sub> decoupling accesses	20/21/22/23/24
RF Out & V <sub>D</sub>	18
GND	1/3/17/19

## Electrical Specifications ( Test Under Probes )

**Test conditions unless otherwise noted:**

- $T_{amb.} = +25^{\circ}\text{C}$
- $V_D = +8\text{V}$
- $V_{G1} = 0\text{V}$
- $V_{G2} = +2\text{V}$

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		45	Ghz
NF	Noise figure		4.5		dB
G	Small signal gain		11		dB
$\Delta G$	Small signal gain flatness		+/-1		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
P1dB	Output P1dB	11	14		dBm
$P_{SAT}$	Saturated output power		17		dBm
$I_D$	Drain current		100		mA

## Environmental parameters

Symbol	Parameter	Values	Unit
Top	Operating temperature range	-40/+85	$^{\circ}\text{C}$
Tstg	Storage temperature range	-55/+85	$^{\circ}\text{C}$

## Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_D$	Drain bias voltage		+9	V
$V_{G2}$	Gate control input access for second stage	-1	$V_D/2$	V
$V_{G1}$	Gate control input access for first stage	-1.5	+0.15	V
$P_{in}$	RF input power		20	dBm
$P_{cw}$	Continuous power dissipation		1	W
T process	Temperature process max 20 seconds		325	$^{\circ}\text{C}$

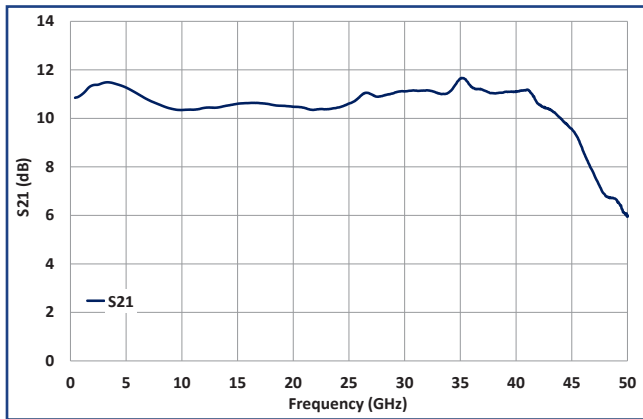
Operation of this device above any of these parameters may cause permanent damage.

## Typical Performances (Test Under Probes)

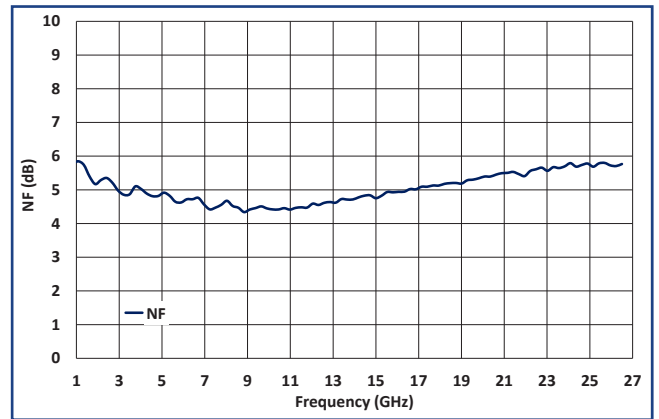
**Measured assembly:** see assembly diagram (except for RF Input and RF Output pads)

- $T_{amb.} = +25^{\circ}\text{C}$
- $V_D = +8\text{V}$
- $I_D = 100\text{mA}$
- $V_{G1} = 0\text{V}$
- $V_{G2} = +2\text{V}$

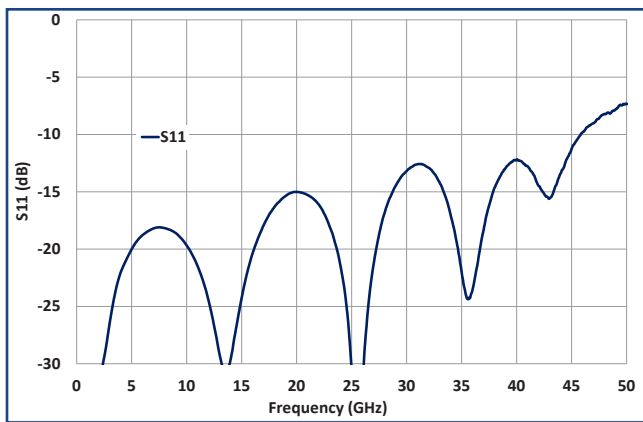
**Small Signal Gain**



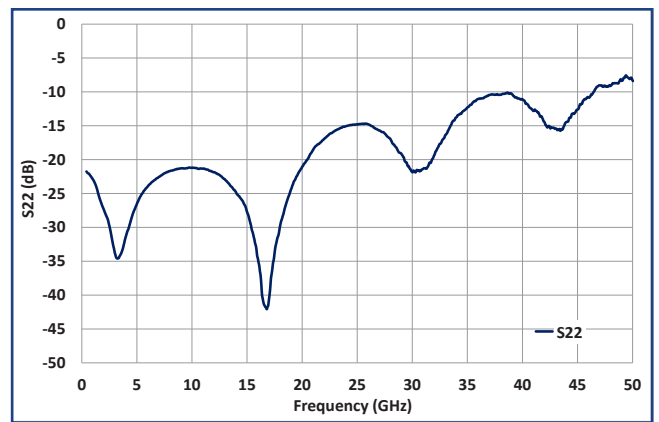
**Noise Figure**



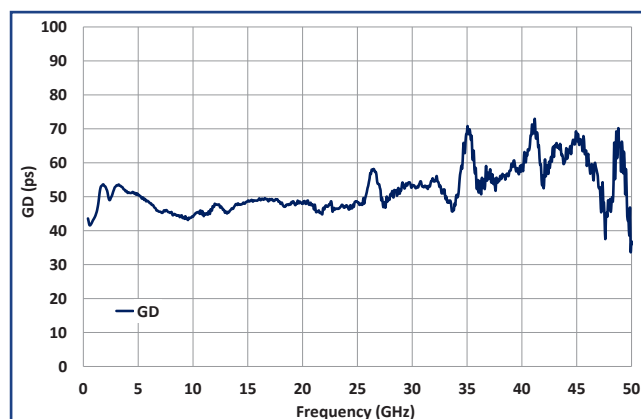
**Input Return Loss**



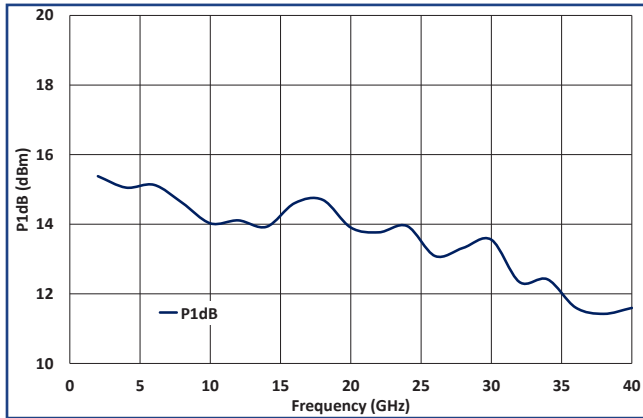
**Output Return Loss**



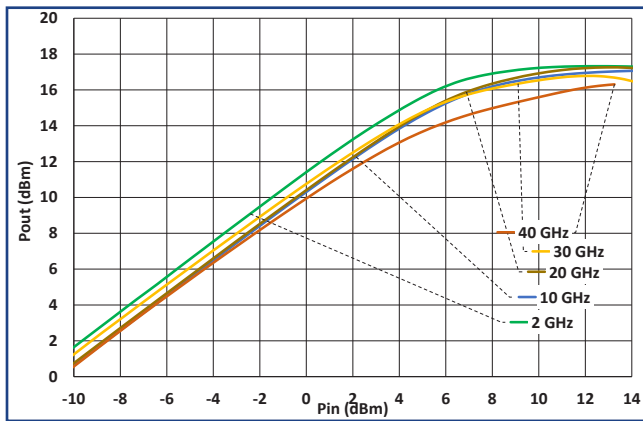
**Group Delay**



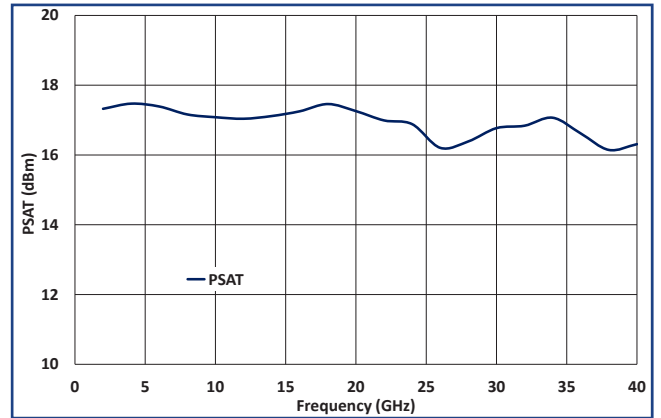
Output P1dB



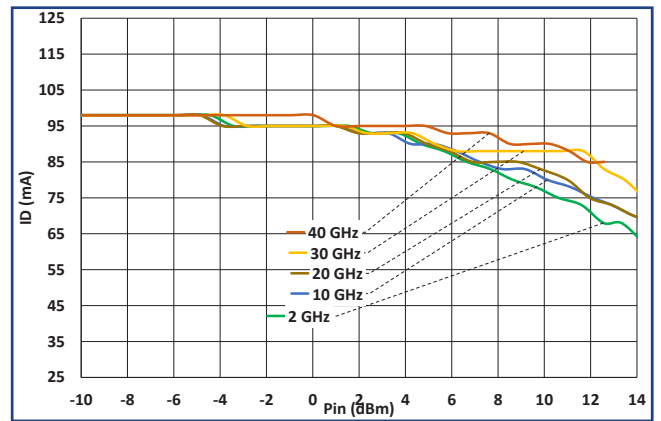
Output Power VS Input Power for various Frequency



Saturated Output Power



Drain Current VS Input Power for various Frequency



**Biasing procedure**

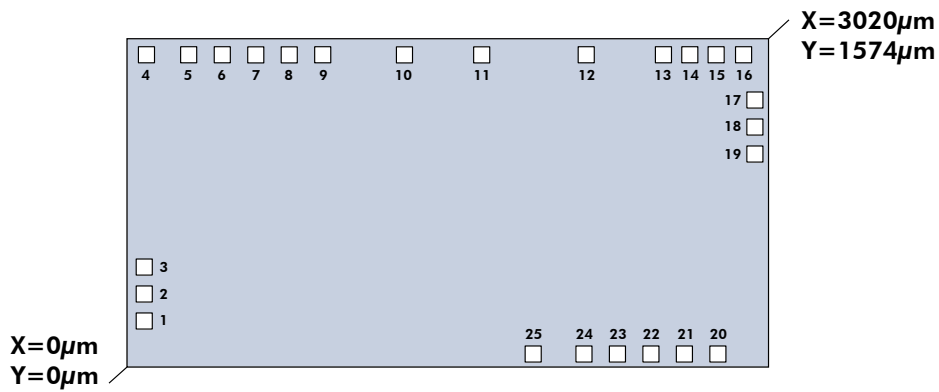
**Switch on**

1. Set  $V_D$  to +8V
2. Set  $V_{G2}$  to +2V
3. Turn RF Input ON

**Switch off**

1. Turn RF Input OFF
2. Decrease  $V_{G2}$  to 0V
3. Decrease  $V_D$  to 0V

## Die Layout



## Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	X (µm)	Y (µm)	Size (µm x µm)	Function
1	90	229	75x75	GND
2	90	351	75x75	RF In
3	90	473	75x75	GND
4	91	1463	75x75	V <sub>G2</sub>
5	263	1466	75x75	D0
6	418	1466	75x75	D1
7	578	1466	75x75	D2
8	738	1466	75x75	D3
9	898	1462	75x75	D4
10	1209	1462	75x75	VbDref
11	1600	1462	75x75	Dref
12	2097	1462	75x75	Det Out
13	2454	1462	75x75	Det In
14	2575	1462	75x75	TC Out
15	2698	1462	75x75	RFL
16	2828	1462	75x75	C0
17	2929	1231	75x75	GND
18	2929	1109	75x75	RF Out & V <sub>D</sub>
19	2930	978	75x75	GND
20	2720	100	75x75	G0
21	2565	100	75x75	G1
22	2405	100	75x75	G2
23	2245	100	75x75	G3
24	2088	103	75x75	G4
25	1850	103	75x75	V <sub>G1</sub>

Die thickness = 100µm

Die bottom must be connected to ground (RF and DC)

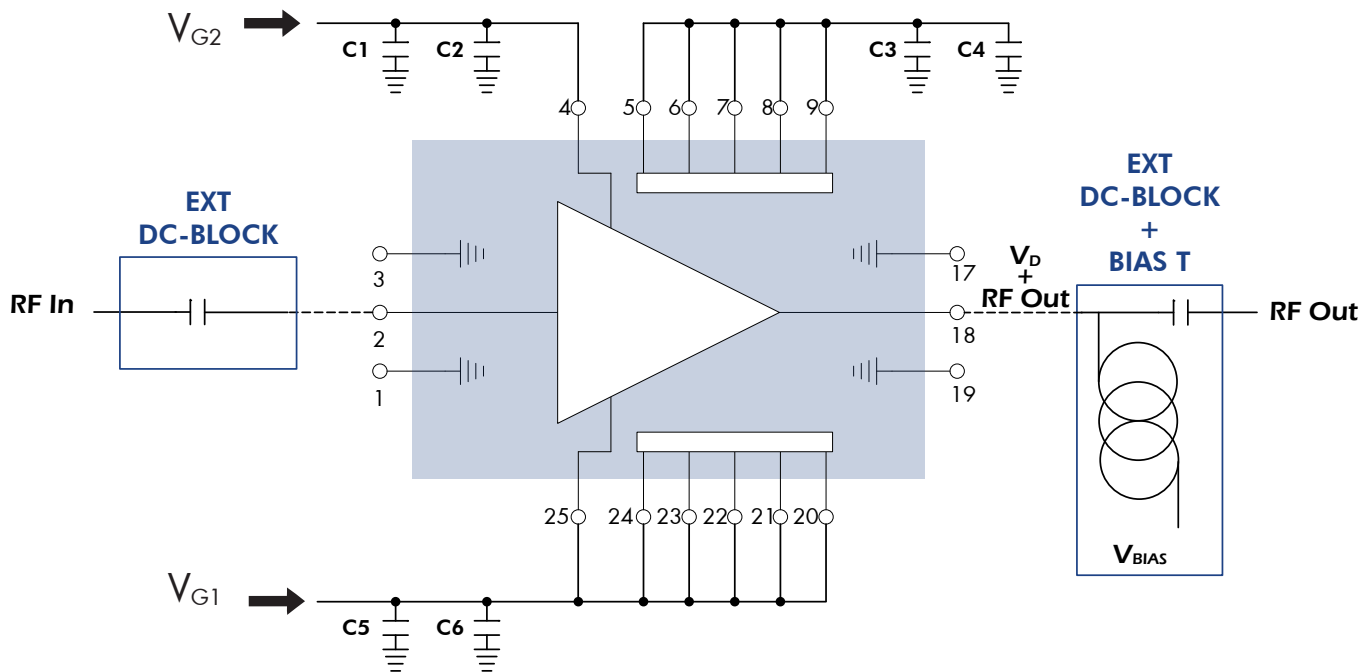
**Access Description**

Pin Number	Name	Description	Electrical interface
2	RF Input	RF Amplifier input, this access is DC coupled and internally matched to 50Ω.	
4	$V_{G2}$	Gate control input access for second stage distributed amplifier structure. Apply +2.5V for nominal biasing conditions.	
5,6,7,8,9	D0 to D4	Decoupling accesses. These 5 accesses must be connected to a same MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire.	
18	RF Output	RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to bias the drain current ( $I_D$ ), by using a wide bandwidth external Bias-T structure.	
25	$V_{G1}$	Gate control input access for first stage distributed amplifier structure. Must be connected to a MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire. It can also be directly connected to the ground reference plane.	
10	VbDref	Reference diode polarization (*)	
11	Dref	Reference diode output (*)	
12	DetOut	Detector output (*)	
13	Det In	Detector input (*)	
14	TC Out	Coupler output, connect to Det I (Pin 13) to use as a detector (*)	
15	RFL	Embedded serial 55Ω serial resistor	
16	C0	Embedded parallel 1pF capacitor	
20,21,22, 23,24	G0 to G4	$V_{G1}$ decoupling accesses. These 5 accesses must be connected to $V_{G1}$	
Die Bottom	GND	Die must be connected to RF and DC Ground	

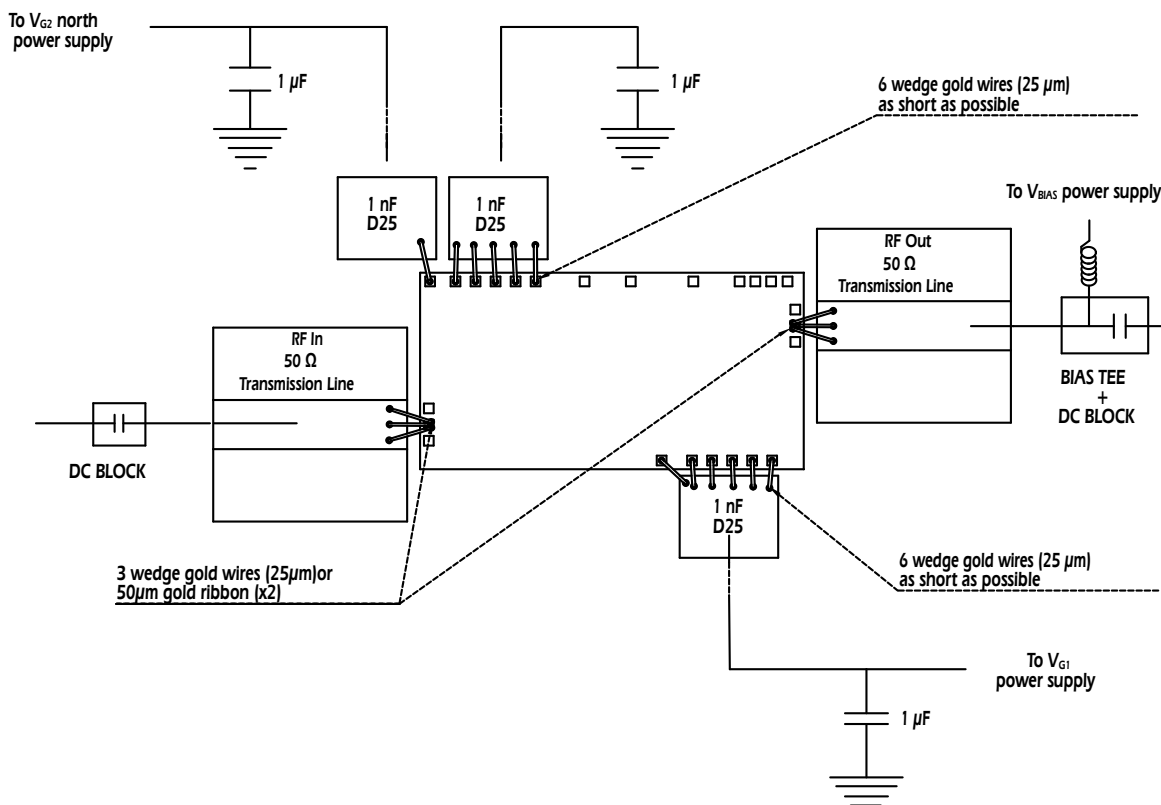
(\*) See application note VWA\_50025\_AAAB\_AN\_Ed1.0.)

## Application Circuit

- C1, C4 and C5 = 1 $\mu$ F
- C2, C3 and C6 1 $\mu$ F capacitors are MIM type and must be placed as close as possible to the die access.



## Typical Assembly Diagram



**Ordering Information**

Product Code	Definition
VWA 5000025AA	DC To 45GHz /11dB / 17dBm

**Associated Material**

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measuments files (S2P)	Contact factory

**Product Compliance Information**

**Solderability :**

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

**ESD Sensitivity Rating :**

Test : Human Body Model (HBM)  
 Standard : JEDEC Standard JESD22-A114



**CAUTION ! ESD-Sensitive device**

**RoHS-Compliance :**

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

**Contact Information**

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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