

General Description

The **VWA500056AA** is a power distributed amplifier designed on a 0.15 μ m pHEMT process. The device is capable of more than +27dBm of output power at saturation regime, and provides more than 15dB of gain from 1 to 20GHz with less than 1dB of flatness with an excellent group delay between 6-18GHz in typical application. The design has been optimized to provide high efficiency, supply current is as low as 290mA with $V_d = +8V$.

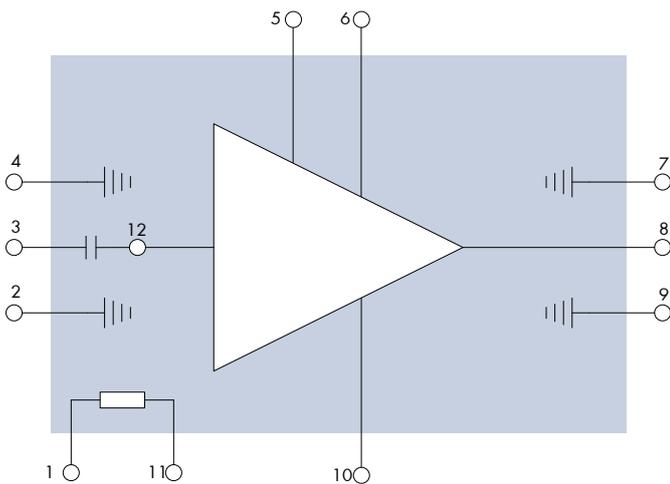
Features

- Distributed amplifier pHEMT GaAs MMIC
- Wide band: 1 to 20GHz.
- Flat group delay
- 50 Ω RF Single ended input and output
- AC coupled In, DC coupled Out
- High Output $P_{sat} > +26dBm$
- Large signal gain: 16dB
- Power supply: 290mA @ +8V
- Chip size: 3 x 1.3 x 0.1 (mm)

Applications

- Wide Band Low Noise Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Broadband / datalink communication

Pins Assignment & Functional Block Diagram



| Symbol | Pad N° |
|----------------|--------|
| RF In | 2 |
| V_{G2} | 5 |
| V_{D_LOAD} | 6 |
| V_D & RF Out | 8 |
| V_G | 10 |
| RA | 1 |
| RB | 11 |
| CA | 12 |

Electrical Specifications

Test conditions unless otherwise noted:

- $T_{amb.} = +25^{\circ}\text{C}$
- $V_{D} = +8\text{V}$
- V_{G1} adjusted between -1V and 0V to obtain Drain current $I_D = 290\text{mA}$
- $V_{G2} = +3\text{V}$

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------|----------------------------|-----|------|-----|------|
| F | Frequency range | 1 | | 20 | GHz |
| G | Small signal gain | 15 | 16 | | dB |
| ΔG | Small signal gain flatness | | +/-1 | | dB |
| NF | Noise figure (@10GHz) | | | 3.5 | dB |
| TOI | Simulated TOI | | 30 | | dBm |
| S11 | Input return loss | | -12 | | dB |
| S22 | Output return loss | | -12 | | dB |
| P1dB | Output P1 dB | | 24 | | dBm |
| P_{SAT} | Saturated output power | | 27 | | dBm |
| I_D | Supply current | | 290 | | mA |

Absolute Maximum Rating

| Symbol | Parameter | Min | Max | Unit |
|----------|--|------|---------|--------------------|
| V_D | Positive External DC bias voltage | | 9 | V |
| V_{G1} | Gate voltage first stage | -2.5 | | V |
| V_{G2} | Gate control input access for second stage | -1 | $V_D/2$ | V |
| Pin max | RF input power (In) | | 18 | dBm |
| P_{cw} | Continuous power dissipation (@ 85 C) | | 3.3 | W |
| T_{st} | Storage temperature | -55 | +85 | $^{\circ}\text{C}$ |
| T_{op} | Operating temperature | -40 | +85 | $^{\circ}\text{C}$ |

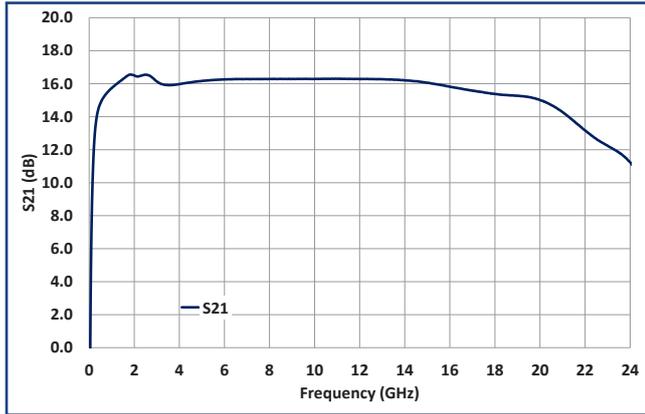
Operation of this device above any of these parameters may cause permanent damage.

Typical Performance (Test under probes)

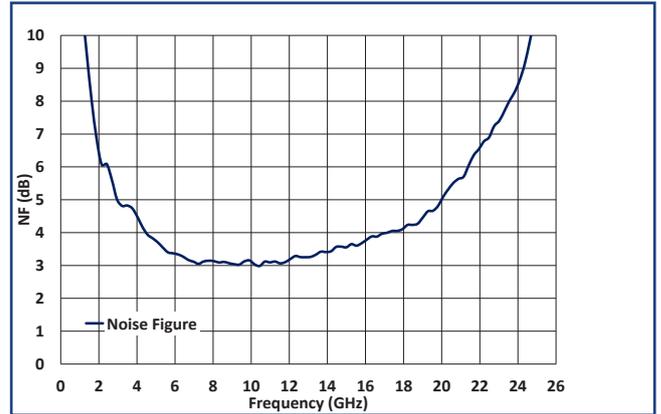
Test conditions unless otherwise noted:

- Tamb.= +25°C
- $V_D = +8V$
- V_{G1} = adjusted between -1V and 0V to obtain $I_D = 290mA$ (without RF Input Signal)
(Typically $V_{G1} = -0.2V$)
- $I_D = 290mA$
- $V_{G2} = +3V$

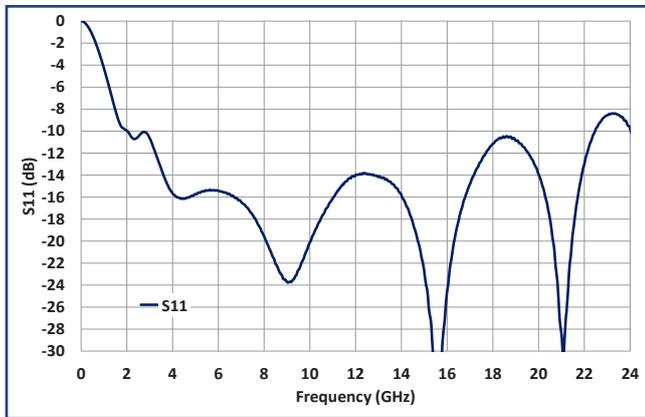
Small Signal Gain



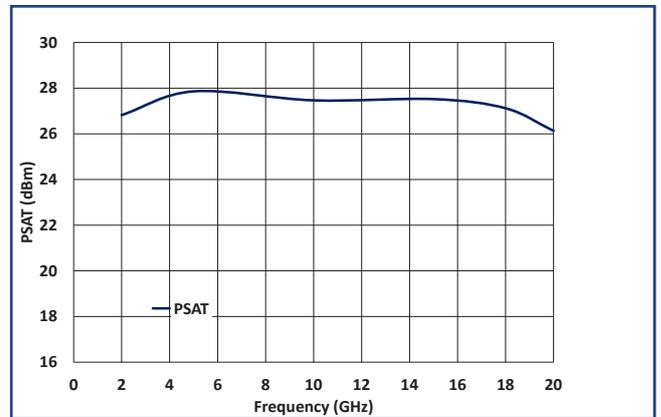
Noise Figure



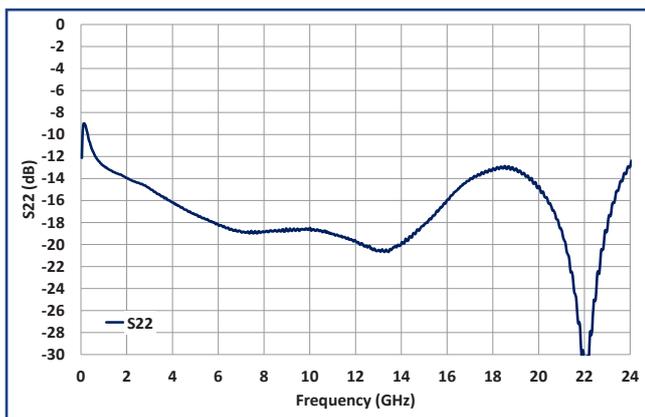
Input Return Loss



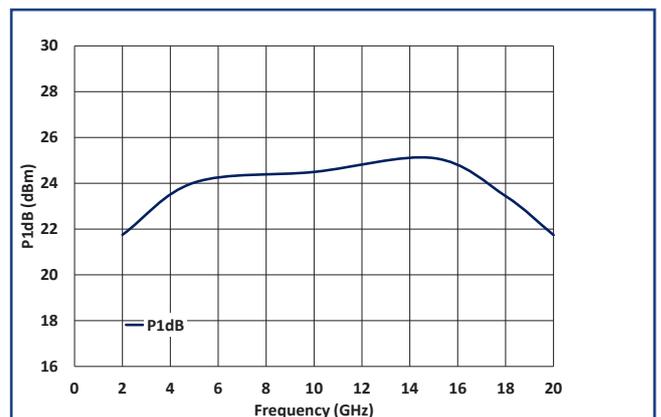
Saturated Output Power



Output Return Loss



Output P1dB

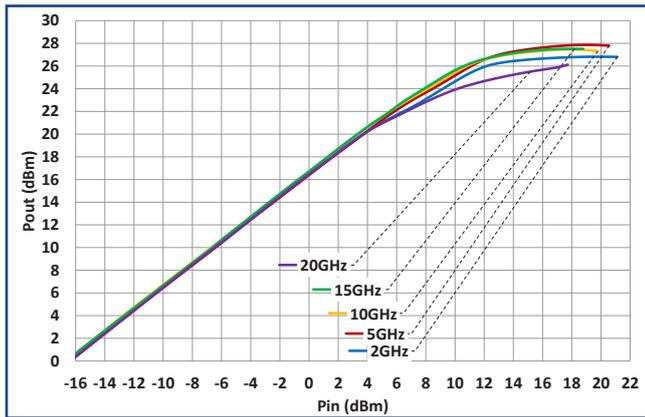


Typical Performance (Test under probes)

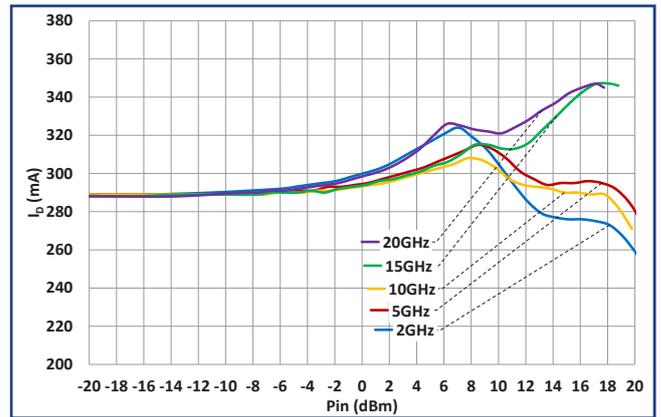
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- $I_D = 290mA$
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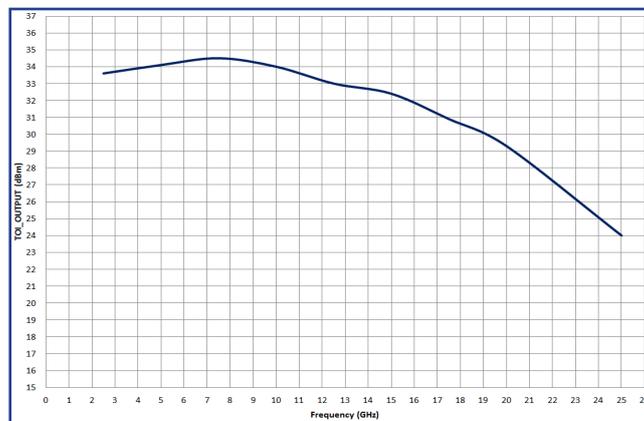
Output Power vs Input Power for various Frequency



Drain Current vs Input Power for various Frequency



SIMULATED Output Third Order Intercept point



Die Layout



Pinout and Bonding Pad Coordinates

| Die Pin Out | | | | |
|-------------|--------|--------|----------------|---------------------|
| Pad | X (µm) | Y (µm) | Size (µm x µm) | Function |
| 1 | 99 | 118 | 75x75 | RA |
| 2 | 99 | 250 | 75x75 | GND |
| 3 | 99 | 400 | 75x75 | RF Input |
| 4 | 99 | 549 | 75x75 | GND |
| 5 | 111 | 787 | 80x100 | V _{G2} |
| 6 | 137 | 1202 | 100x150 | V _{D_LOAD} |
| 7 | 2922 | 1215 | 75x75 | GND |
| 8 | 2922 | 1065 | 75x75 | RF Output |
| 9 | 2922 | 915 | 75x75 | GND |
| 10 | 2909 | 294 | 100x150 | V _{G1} |
| 11 | 292 | 118 | 75x75 | RB |
| 12 | 371 | 400 | 75x75 | CA |

Die thickness = 100µm

Die bottom must be connected to ground (RF and DC)

Access Description

| Pin Number | Name | Description | Electrical interface |
|------------|---------------|---|----------------------|
| 3 | RF In | RF Amplifier input, this access is AC coupled and internally matched to 50Ω. | |
| 5 | V_{G2} | Gate control input access for second stage distributed amplifier structure. Apply +3V for nominal biasing conditions. | |
| 10 | V_{G1} | Gate control input access for first stage distributed amplifier structure. Adjust V_{G1} to obtain the desired Drain current (~0.2V for nominal biasing conditions) | |
| 6 | V_{D_LOAD} | Drain termination load decoupling access. For lower frequency applications, this access can be connected to a MIM 100pF or 1000pF capacitor, with a low inductance connection. | |
| 8 | RF Out | RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to feed the drain current (I_D), by using a wide bandwidth external Bias-T structure. | |
| 1 | RA | Embedded resistor for low frequencies applications. Unused for nominal biasing conditions. | |
| 11 | RB | Embedded resistor for low frequencies applications. Unused for nominal biasing conditions. | |
| Die Bottom | GND | Die must be connected to RF and DC Ground | |

Biasing procedure

Switch on

1. Set V_{G1} to -1V
2. Set V_D to +8V
3. Set V_{G2} to +3V
4. Increase V_{G1} to obtain $I_D = 290\text{mA}$ (typically $V_G = -0.2\text{V}$)
5. Turn RF Input ON

Switch off

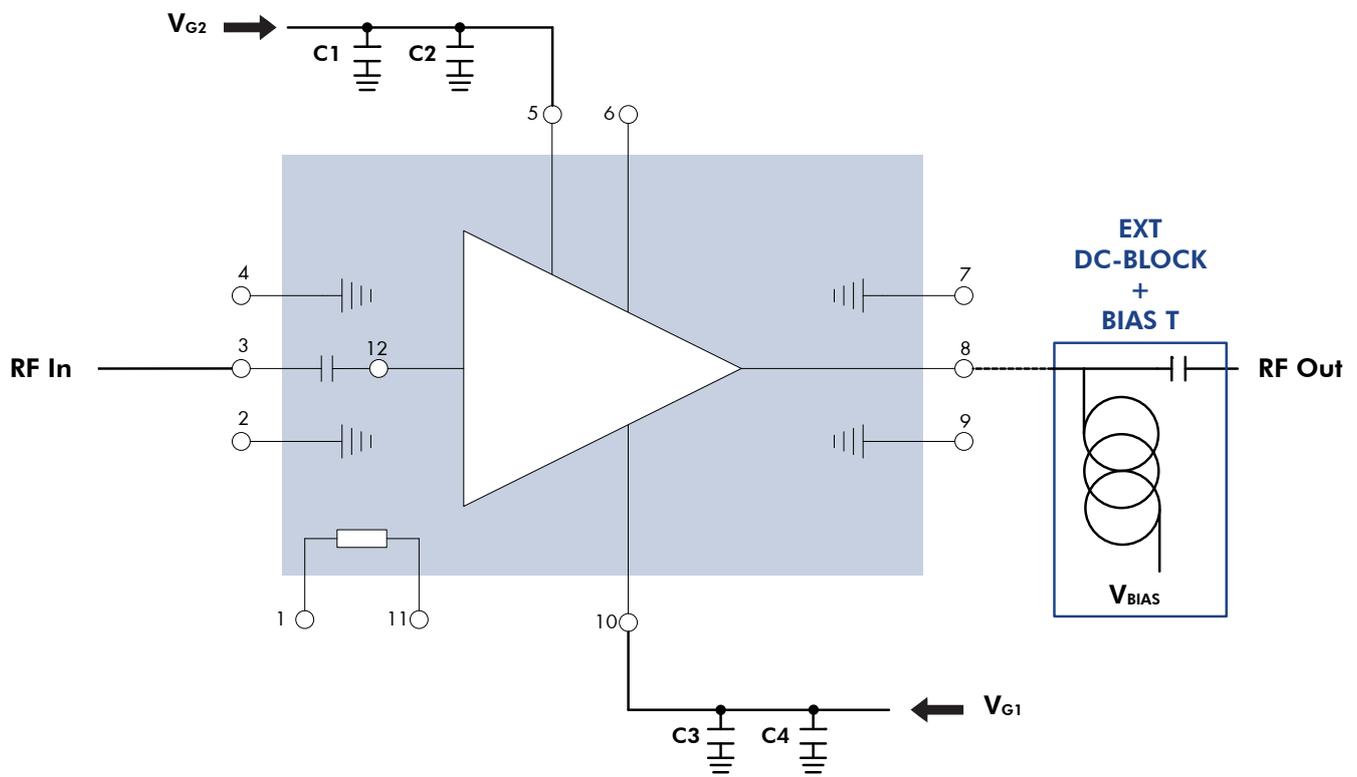
1. Turn RF Input OFF
2. Decrease V_{G1} to -1V
3. Set V_{G2} to 0V
4. Set V_D to 0V
5. Set V_{G1} to 0V



- Always apply V_{G1} before applying V_D
- This stress may cause permanent damage on component.

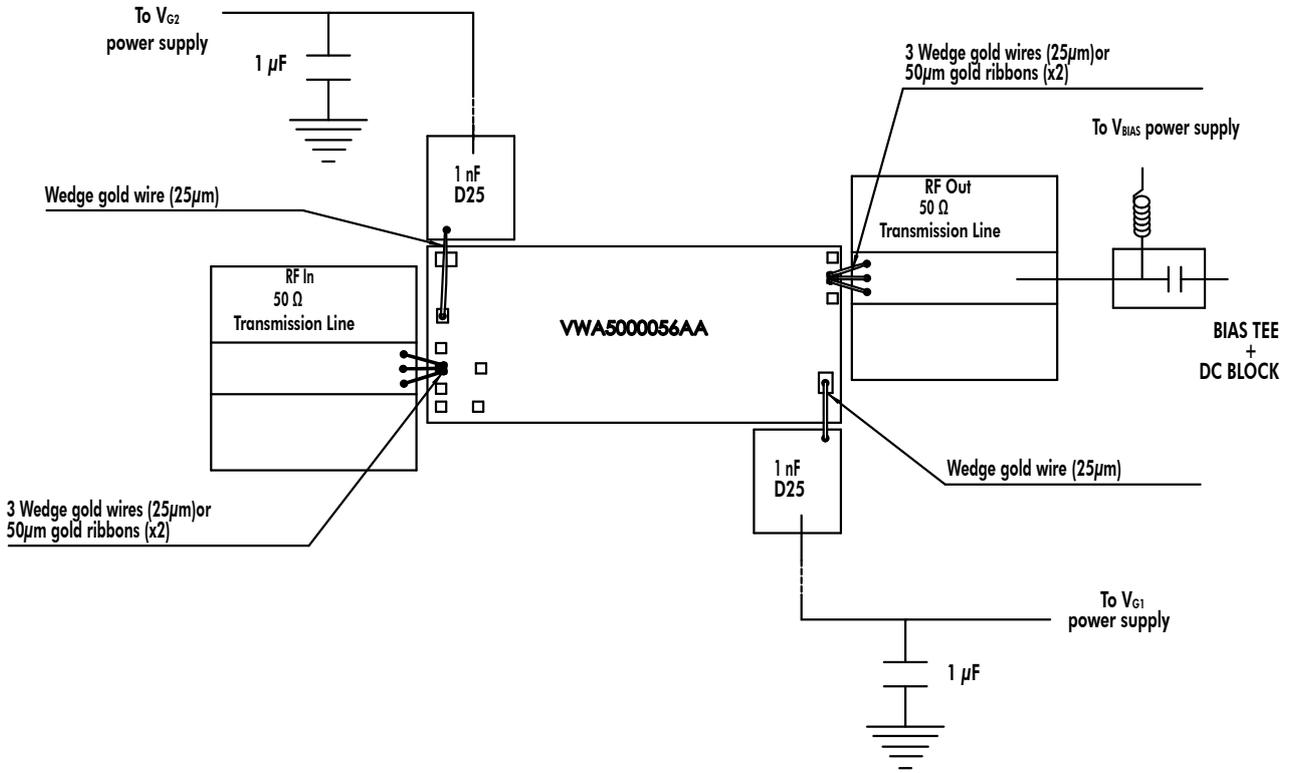
Application Circuit

- C1 and C4: 1 μF
- C2 and C3: 1nF capacitors are MIM type and must be placed as close as possible to the die access.

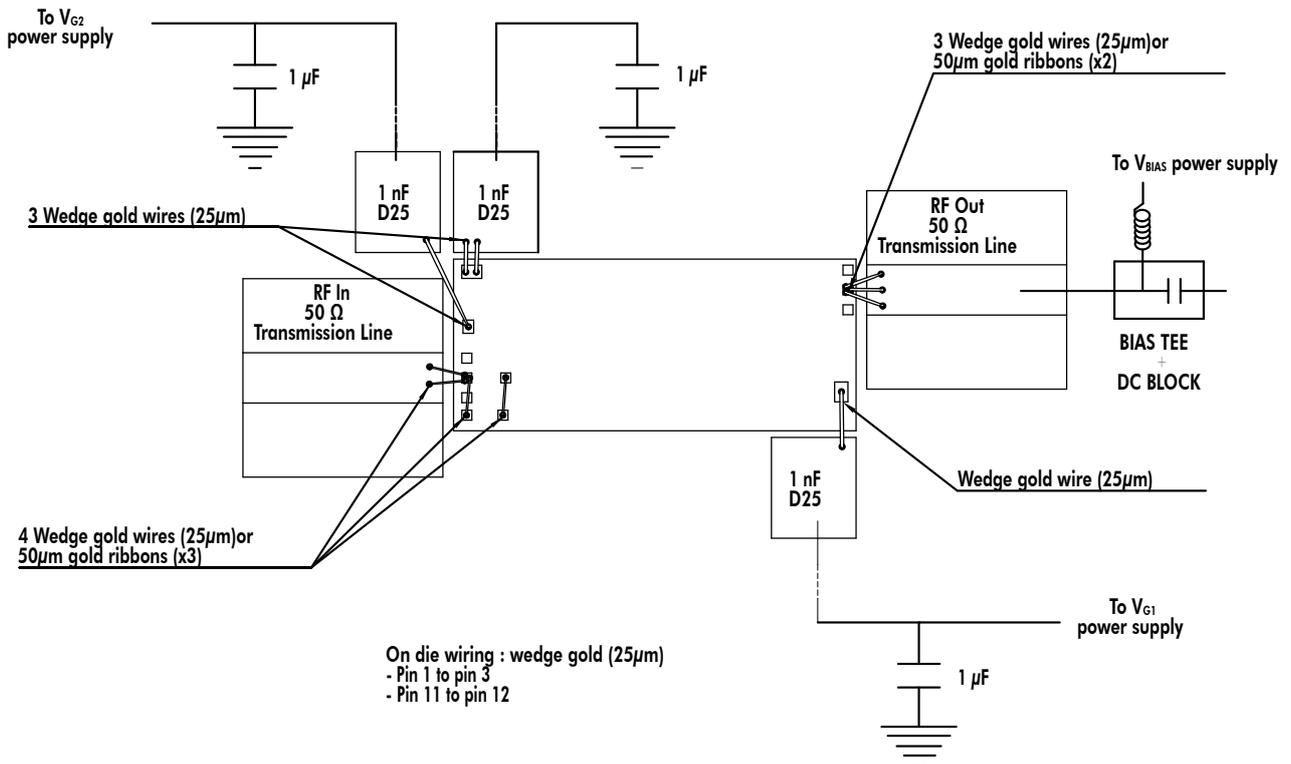


Assembly diagram

Typical application



Low frequency application



Ordering Information

| Product Code | Definition |
|---------------|---------------------------|
| VWA 5000056AA | 1 to 20GHz / 16dB / 27dBm |

Associated Material

| Material | Status |
|--|-----------------|
| Packaged die | Contact factory |
| Die Evaluation Board (die EVB) | Contact factory |
| Packaged die Evaluation Board (packaged die EVB) | Contact factory |
| Mechanical files (DXF) | Contact factory |
| Measurements files (S2P) | Contact factory |

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivity Rating :

Test : Human Body Model (HBM)
 Standard : JEDEC Standard JESD22-A114



CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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