

## General Description

The **VWA500061AA** is a gain block amplifier designed on a 0.15µm pHEMT process.

The device delivers +15.5dBm of output power at saturation regime and more than +13.5dBm of output power at 1dB of gain compression. It provides a 0.2dB flat 13dB of linear gain from 8.5GHz to 12GHz. The supply current is 70mA when operating with a single power supply  $V_D = +5V$ .

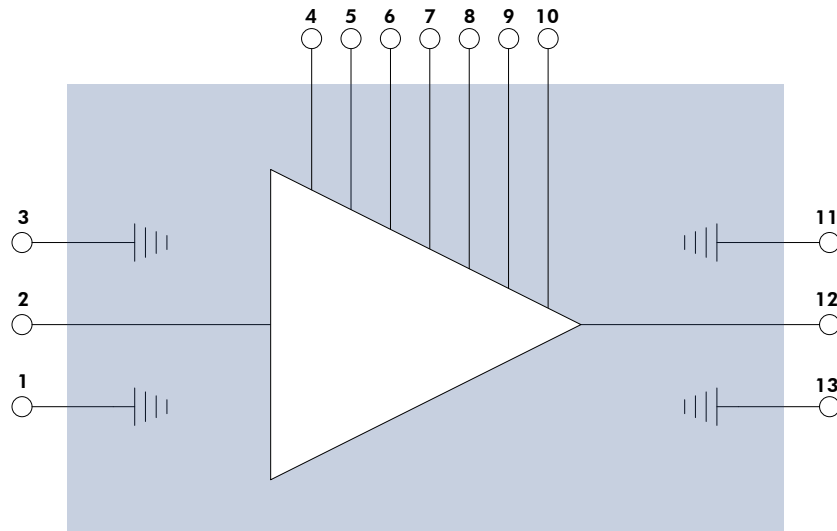
## Features

- Block amplifier pHEMT GaAs MMIC
- Wide band: 8.5 to 12GHz.
- 50ΩRF Ac coupled input and output
- P1dB >+13.5dBm
- Output Psat >+15.5dBm
- Small signal gain: 13dB from 8.5GHz to 12GHz
- Power supply: 70mA @ +5V
- Chip size: 2.27 x 2.97 x 0.1 (mm)

## Applications

- Wide band MPA
- Radar / ECM / ECCM
- Test and measurement
- Broadband / datalink communication

## Pins Assignement & Functional Block Diagram



Symbol	Pad N°	Symbol	
RF In	2	$V_{D1\_E}$	8
$V_{D1\_A}$	4	$V_{D2\_A}$	9
$V_{D1\_B}$	5	$V_{D2\_B}$	10
$V_{D1\_C}$	6	RF Out	12
$V_{D1\_D}$	7	GND	1/3/11/13

## Electrical Specifications

**Test conditions unless otherwise noted:**

- Tamb.= +25°C
- $V_D = V_{D1\_E} = V_{D2\_A} = +5V$

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency Range	8.5		12	GHz
NF	Simulated Noise figure		3		dB
G	Small signal gain	13	13.5		dB
$\Delta G$	Small-signal Gain flatness		+/-0.1	+/-0.2	dB
S11	Input return loss		-12	-9.5	dB
S22	Output return loss			-15	dB
P1dB	Output P1dB	13.5	14.5		dBm
$P_{SAT}$	Saturated output power	15.5	16		dBm
$I_D$	Total Drain Current ( $I_D = I_{D1\_E} + I_{D2\_A}$ )		70		mA

## Environmental parameters

Symbol	Parameter	Values	Unit
Ta	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+85	°C

## Absolute Maximum Ratings

Symbol	Parameter	Values (max)	Unit
$V_D$	Positive external DC bias voltage	7	V
Pin	RF input power (In)	12	dBm
Tj	Junction temperature	150	°C
Pcw	Continuous power dissipation (@85 °C)	0.6	W
T process	Temperature process max 20 seconds	325	°C

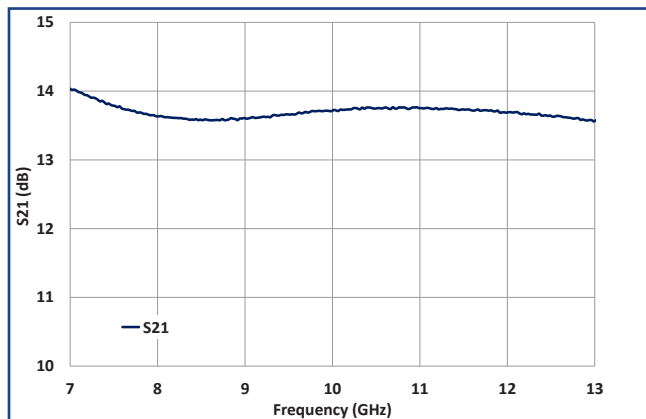
Operation of this device above any of these parameters may cause permanent damage.

## Typical Performance ( Test Under Probes)

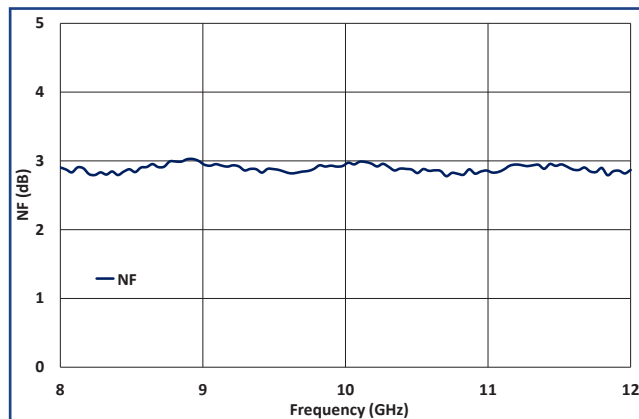
**Test conditions unless otherwise noted:**

- $T_{amb.} = +25^{\circ}C$
- $V_D = V_{D1\_E} = V_{D2\_A} = +5V$
- $I_D = I_{D1\_E} = I_{D2\_A} = 70\text{ mA}$

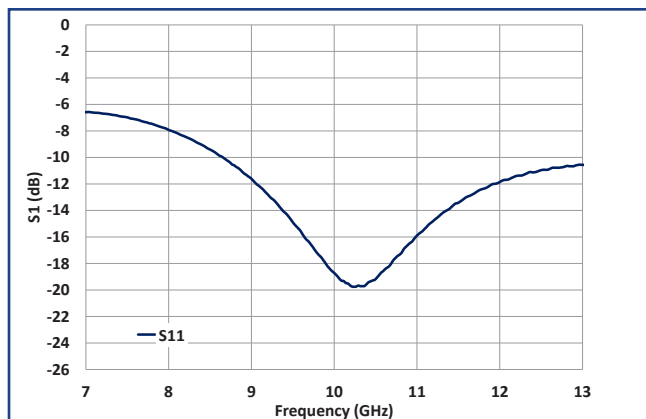
**Small Signal Gain**



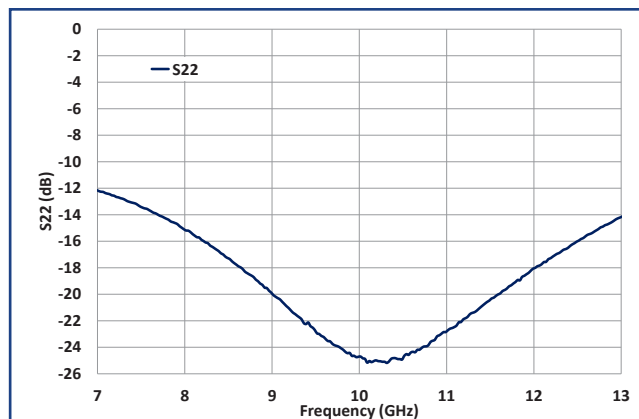
**Noise Figure**



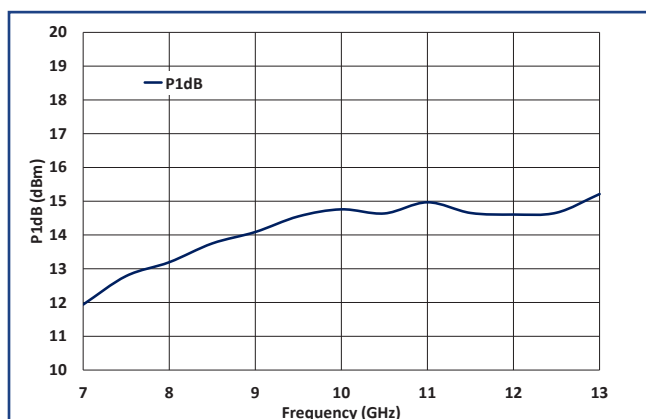
**Input Return Loss**



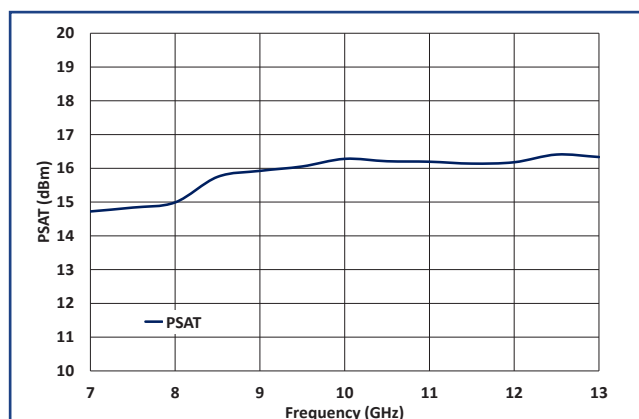
**Output Return Loss**



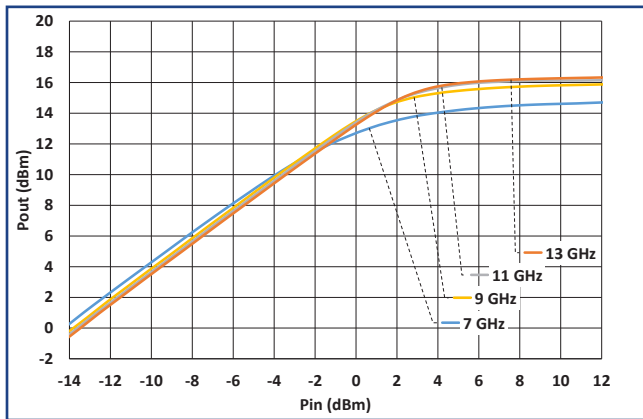
**Output P1dB**



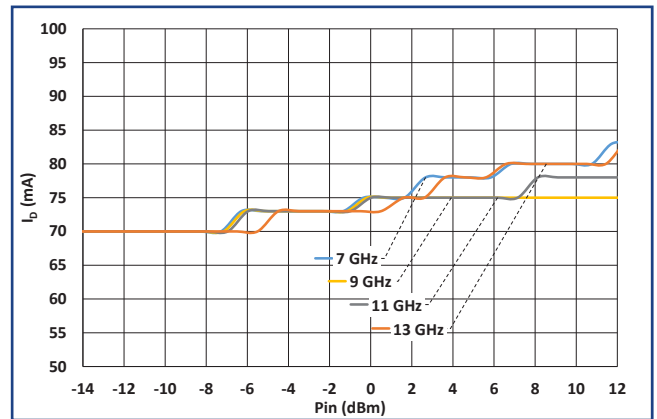
**Saturated Output Power**



Output Power vs Input Power for various Frequency



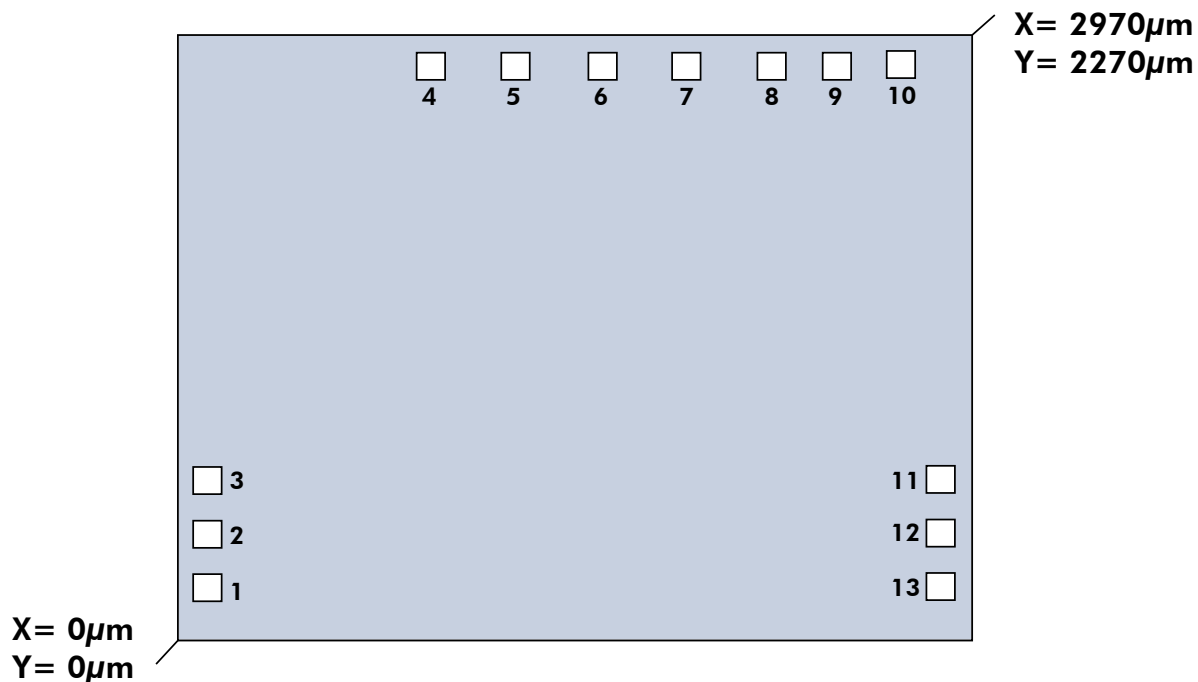
$I_D$  vs Input Power for various Frequency



### Access Description

Pin Number	Name	Description	Electrical interface
2	RF Input	AC coupled, amplifier input access	
12	RF Output	AC coupled amplifier output access.	
4	$V_{D1\_A}$	1rst stages drain biasing access	
5	$V_{D1\_B}$	1rst stages drain biasing access through a 25Ω serial resistor.	
6	$V_{D1\_C}$	1rst stages drain biasing access through a 50Ω serial resistor.	
7	$V_{D1\_D}$	1rst stages drain biasing access through a 50Ω serial resistor.	
8	$V_{D1\_E}$	1rst stages drain biasing access through a 100Ω serial resistor.	
9	$V_{D2\_A}$	2nd stage drain biasing access through a 25Ω serial resistor.	
10	$V_{D2\_B}$	2nd stage drain biasing access.	
Die Bottom	GND	Die must be connected to RF and DC Ground	

## Die Layout



## Pinout and Bonding Pad Coordinates

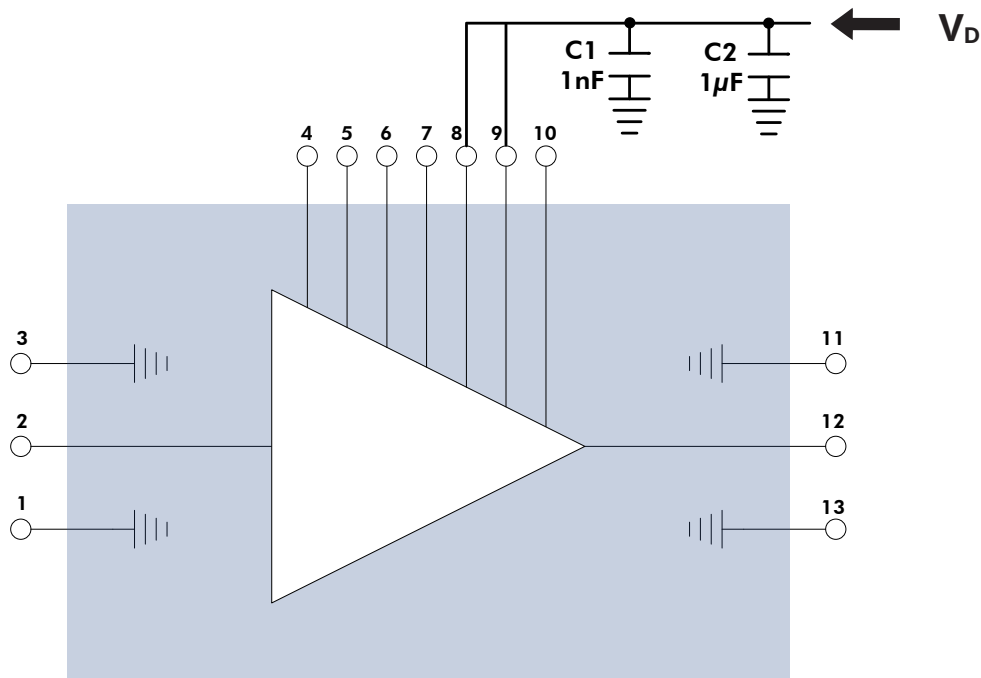
Die Pin Out				
Pad	X (µm)	Y (µm)	Size (µm x µm)	Function
1	107	202	100x100	GND
2	107	403	100x100	RF In
3	107	603	100x100	GND
4	944	2162	100x100	V <sub>D1_A</sub>
5	1262	2162	100x100	V <sub>D1_B</sub>
6	1581	2162	100x100	V <sub>D1_C</sub>
7	1899	2162	100x100	V <sub>D1_D</sub>
8	2218	2162	100x100	V <sub>D1_E</sub>
9	2459	2162	100x100	V <sub>D2_A</sub>
10	2704	2162	100x100	V <sub>D2_B</sub>
11	2850	602	100x100	GND
12	2850	403	100x100	RF Out
13	2850	202	100x100	GND

Die thickness = 100µm

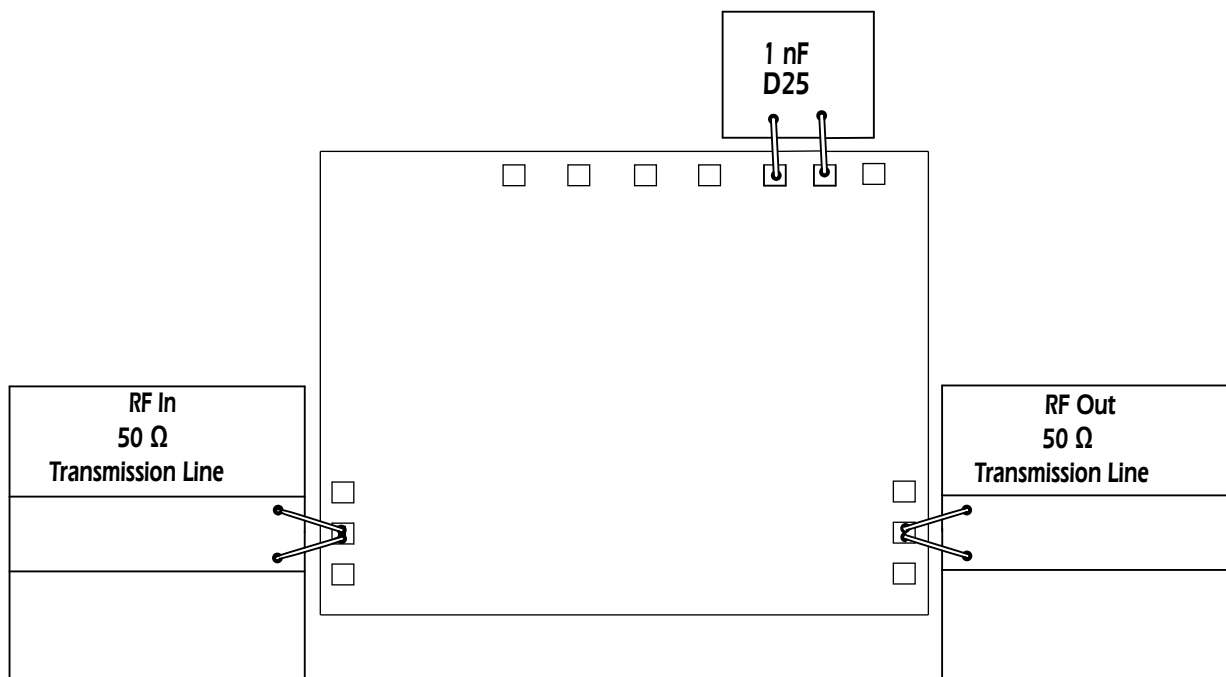
Die bottom must be connected to ground (RF and DC)

## Application circuit

- C1= 1nF Should be Mim capacitors close to the die
- C2= 1μF



## Typical Assembly Diagram



## Ordering Information

Product Code	Definition
VWA 5000061 AA	8.5 to 12GHz / 13dB / 16dBm

## Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurements files (S2P)	Contact factory

## Product Compliance Information

### Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

### ESD Sensitivity Rating :

Test : Human Body Model (HBM)  
 Standard : JEDEC Standard JESD22-A114



**CAUTION ! ESD-Sensitive device**

### RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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