DC to 50GHz / 10dB Gain / 20dBm P_{SAT} Wideband Distributed Amplifier Internal Active Bias-Tee

DATA SHEET | **PRELIMINARY** | **VWA 5000078 AA**

General Description

The **VWA5000078AA** is a wideband distributed amplifier designed on a 0.15µm pHEMT process.

The device is capable of more than +19dBm of output power at saturation regime, up to 50GHz and more than +16dBm of output power at 1dB of gain compression, up to 30GHz. It provides more than 10dB of linear gain from DC to 50 GHz with a positive slope up to 50GHz when operating with V_D= +8V, with an excellent group delay. The design integrates an internal active drain biasing system that allows to avoid external Bias-Tee structure to feed the drain current. The supply current is as low as 135mA when operating with V_D= +8V.

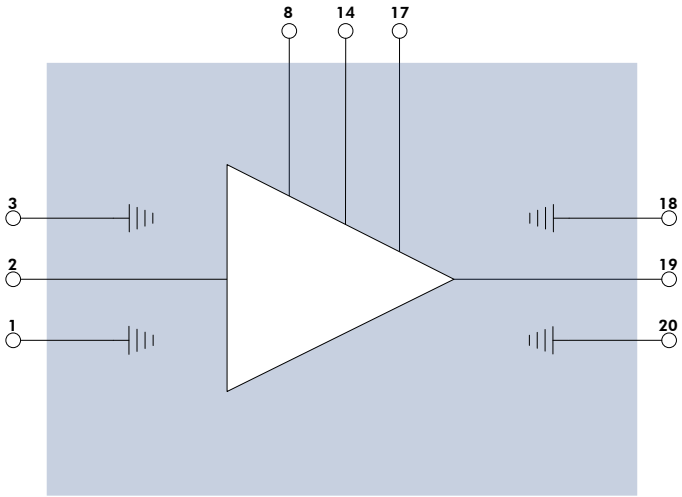
Features

- Distributed amplifier pHEMT GaAs MMIC
- Wide band: DC to 50GHz
- Internal Active Drain Biasing System
- Flat group Delay
- 50ΩRF Single ended input and output
- DC coupled IN, DC coupled Out
- P1dB >+16dBm DC to 30GHz
- High output Psat: +20dBm (typical)
- Small signal gain: >10dB from DC to 50GHz
- Power supply: 135mA @ +8V
- Chip size: 2.3 x 1.8 x 0.1 (mm)

Applications

- Radar / ECM / ECCM
- Wide band MZM Driver: N(RZ), PAMX, QPSK
- Test and measurement
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Symbol	Pad N°
RF In	2
V_{G2}	8
Decoupling Cap A	14
V_D	17
RF Out	19
GND	1, 3, 18, 20

Electrical Specifications

Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D = +8V
- I_D= 135mA
- V_{G2} = +2.5V
- V_{G2} linked to decoupling Cap A (pad 8 linked to pad 14)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency Range	DC		50	GHz
G	Small signal gain	10	11		dB
ΔG	Small signal gain flatness		+/-1		dB
+ ΔG	Average gain positive slope		0.06		dB/GHz
S11	Input return loss		-12	-6	dB
S22	Output return loss		-15	-9	dB
NF	Noise figure (1 to 26.5GHz)		5		dB
OP_{1dB}	Output P1dB (DC to 44GHz)		16		dBm
P_{SAT}	Saturated output power		20		dBm

Recommended Operating Conditions

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	8	V
I_D	Drain bias current	135	mA
V_{G2}	Gate bias voltage	2.5	V

Absolute Mawimum Ratings

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	9	V
V_{G2}	Gate bias voltage	V_D/2	V
Pin	Maximum peak input power overdrive	20	dBm
P_{DISS}	Power dissipation	1.4	W
Tj	Junction temperature	150	°C
Ta	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-45/+125	°C

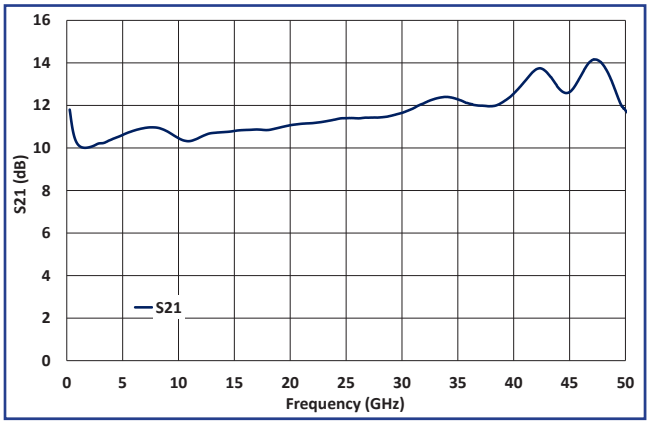
Operation of this device above any of these parameters may cause permanent damage.

Typical Performance (Small Signal / Test Under Probes)

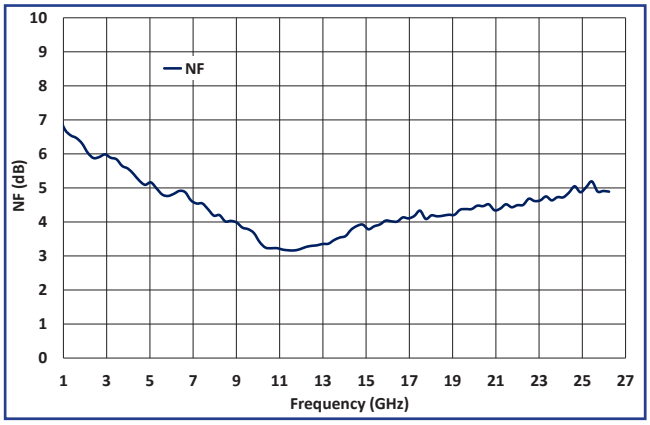
Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D = +8V, I_D= 135mA
- Pin= -20dBm
- V_{G2} = +2.5V
- V_{G2} linked to decoupling Cap A (pad 8 linked to pad 14)

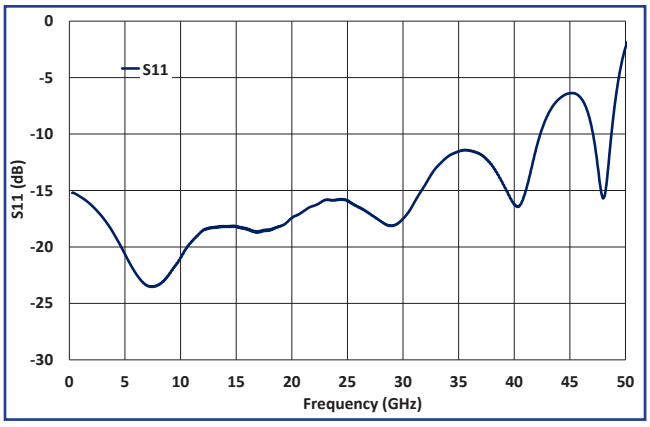
Small Signal Gain



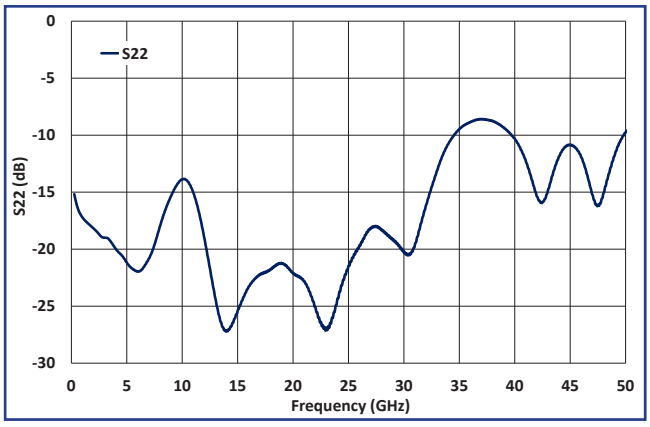
Noise Figure



Input Return Loss



Output Return Loss

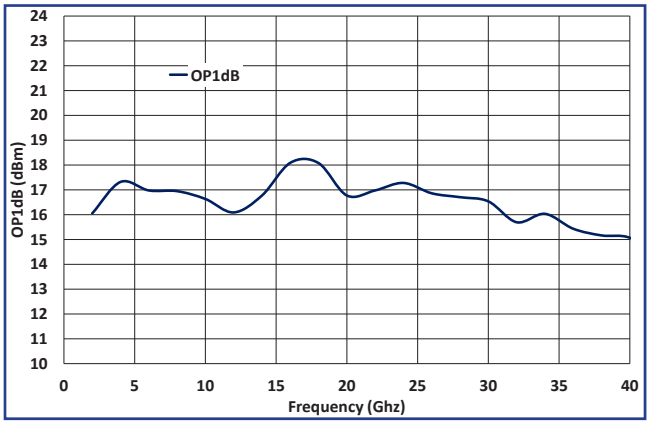


Typical Performance (Power Measurement / Test Under Probes)

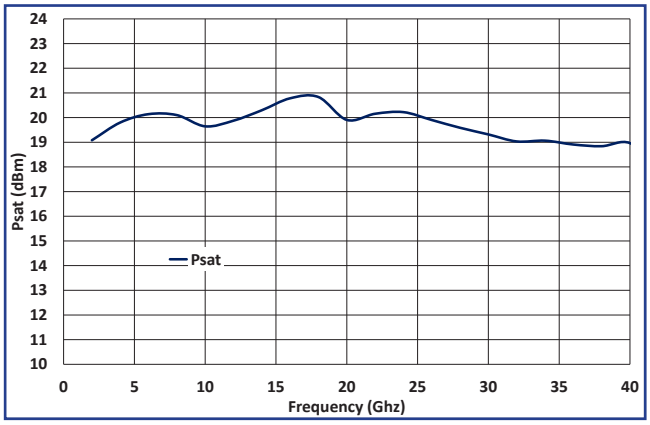
Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D = +8V, I_D= 135mA
- V_{G2} = +2.5V
- V_{G2} linked to decoupling Cap A (pad 8 linked to pad 14)

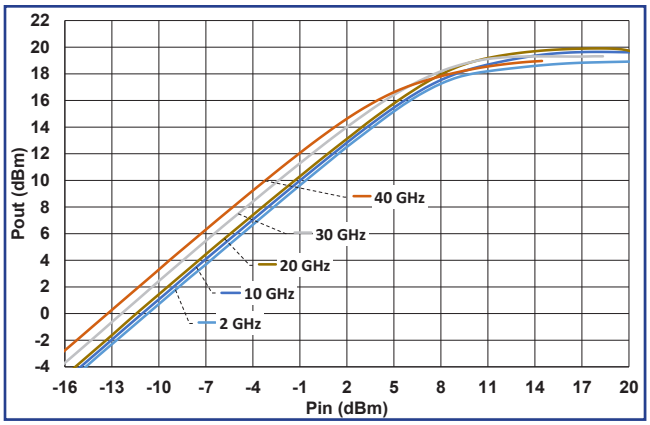
Ouput P1dB



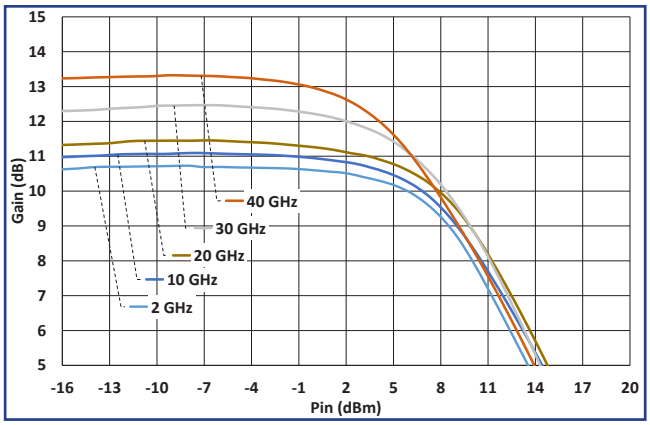
Saturated Output Power



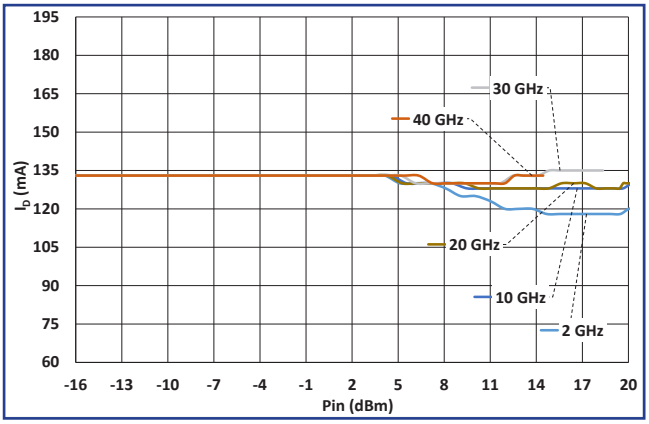
Output Power vs Input Power for various Frequency



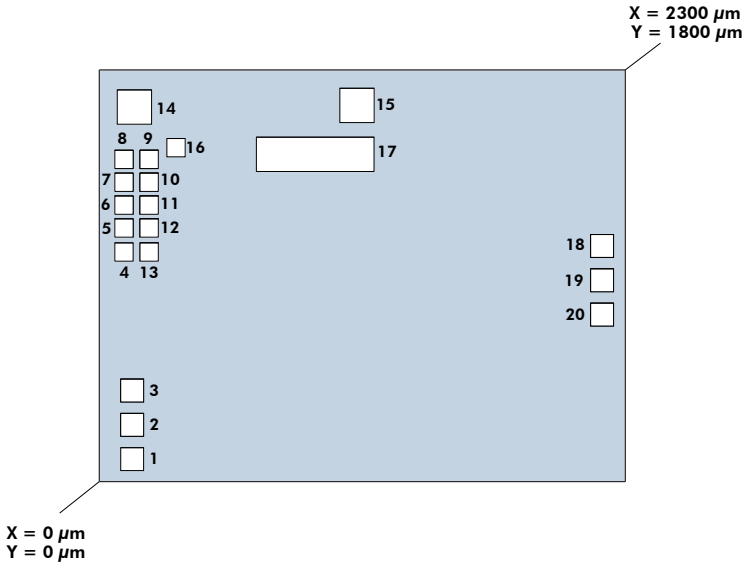
Power Gain vs Input Power for various Frequency



Drain Current vs Input Power for various Frequency



Die Layout



Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	145	98	100x100	GND
2	145	248	100x100	RF In
3	145	398	100x100	GND
4	108	1000	80x80	V_{G2}
5	108	1100	80x80	V_{G2}
6	108	1200	80x80	V_{G2}
7	108	1300	80x80	V_{G2}
8	108	1400	80x80	V_{G2}
9	218	1400	80x80	V_{BIAS}_1
10	218	1300	80x80	V_{BIAS}_2
11	218	1200	80x80	V_{BIAS}_3
12	218	1100	80x80	V_{BIAS}_4
13	218	1000	80x80	V_{BIAS}_5
14	150	1640	150x150	Decoupling Cap A
15	1130	1645	150x150	Decoupling Cap B
16	335	1460	80x80	V_{BIAS}_6
17	944	1430	515x150	V_D
18	2198	1030	100x100	GND
19	2198	880	100x100	RF Out
20	2198	730	100x100	GND

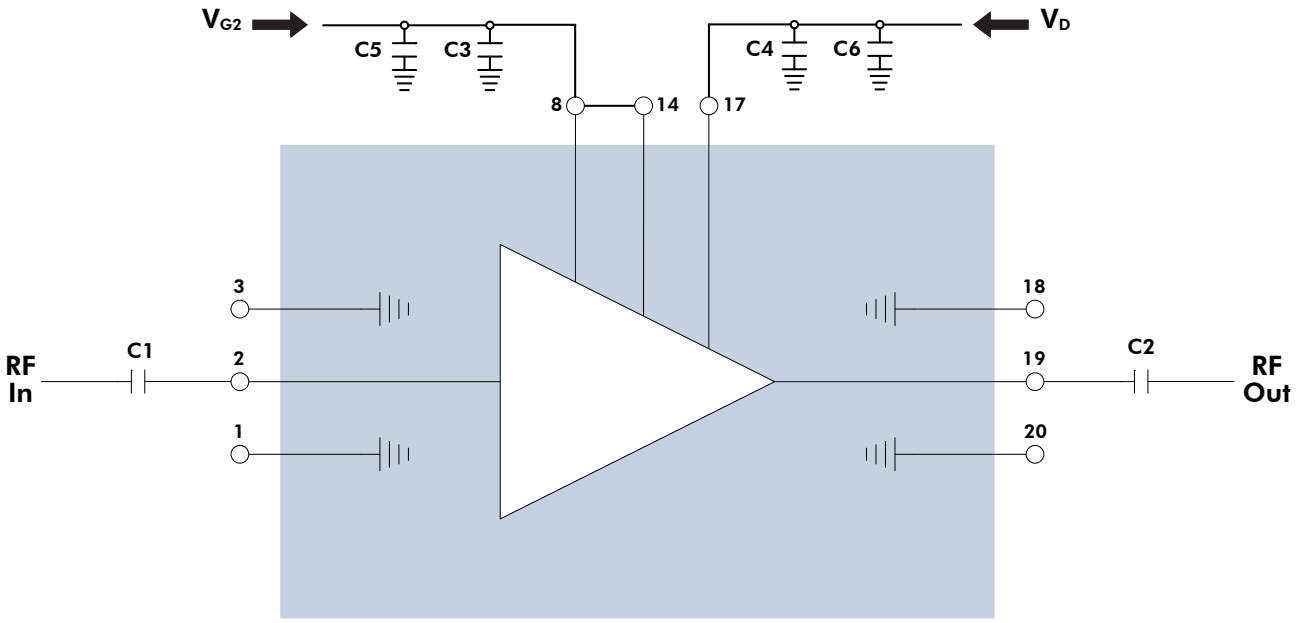
Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

Application Circuit

Components:

- C1, C2: external DC-BLOCK
- C3, C4: 1nF
- C5, C6: 1µF
- PAD 8 to PAD 14 link : wire bond
- PAD 1, 3, 18, 20 to GND: wire bond

C3 and C4 should be MIM capacitors and must be placed as close as possible to the die access.



Bias-up Procedure

1. Apply V_D= +8V
2. Apply V_{G2}= +2.5V
3. Apply RF signal in pulsed mode

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_{G2} to 0V
3. Reduce V_D= 0V
4. Turn off power supply

Ordering Information

Product Code	Definition
VWA 5000078 AA	DC To 50GHz / 10dB Gain / 20dBm P_{SAT}

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

Vectrawave SA
5, rue Louis de Broglie
22 300 Lannion
France

www.vectrawave.com
Email sales: contact_sales@vectrawave.com
Tel sales:+33 (0)2 57 63 00 20

Represented by