

VM087D (old ref.: VWA 5000087 AB)

• General Description

The VM087D is a Microwave Monolithic Integrated Circuit (MMIC) designed in HEMT (High Electron Mobility Transistor) structure for operating frequency range from 7.5 to 8.5GHz.

The MMIC is developed on 250nm GaN/SiC process and is internally matched through 50Ω RF accesses. It can provide an output power up to 40W and associated power added efficiency of 39% in pulsed mode.

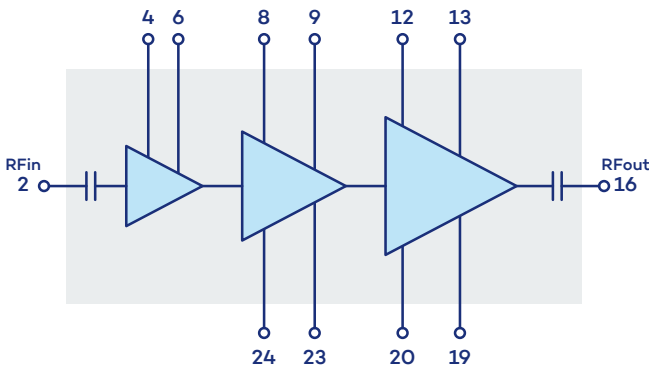
• Features

Frequency range	7.5 – 8.5GHz
Output Power	46dBm @Pin = 25dBm
PAE	39% @Pin = 25dBm
Linear Gain	29dB
DC bias	V_D = +28V, I_{DQ} = 320mA, (V_G = -2.4V Typical)
Chip size	4 x 4.8 x 0.1 (mm)

• Applications

- Radar
- Test and Measurement
- Communication

• Pins Assignment & Functional Block Diagram



Function	Pin number
RFin	2
V _{G1}	4
V _{D1}	6
V _{G2}	8/24
V _{D2}	9/23
V _{G3}	12/20
V _{D3}	13/19
RFout	16

• Electrical Specifications

Test conditions: unless otherwise noted

- $T_{amb} = +25^{\circ}\text{C}$
- $V_D = +28\text{V}$
- $I_{DQ} = 320\text{mA}$ ($V_G = -2.4\text{V Typ.}$)
- Pulsed mode (pulse width: $30\mu\text{s}$, duty cycle: 10%)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	7.5		8.5	GHz
G	Linear gain		29		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
P _{out}	Output power (@P _{in} =25dBm)		46		dBm
PAE	Associated Power Added Efficiency (@P _{in} =25dBm)		39		%
I _D	Associated Drain current (@P _{in} =25dBm)		4		A
V _D	Drain voltage		28		V

• Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V _D	Drain voltage	28	V
I _{DQ}	Drain quiescent current	320	mA
V _G	Gate voltage	-2.4 (Typ.)	V

• Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _D	Drain bias voltage	35	V
I _D	Drain bias current	5,5	A
V _G	Gate bias voltage	-10 to -2	V
P _{in}	Maximum peak input power overdrive	30	dBm
T _j	Junction temperature	225	°C
T _a	Operating temperature range	-40/+85	°C
T _{stg}	Storage temperature range	-55/+150	°C

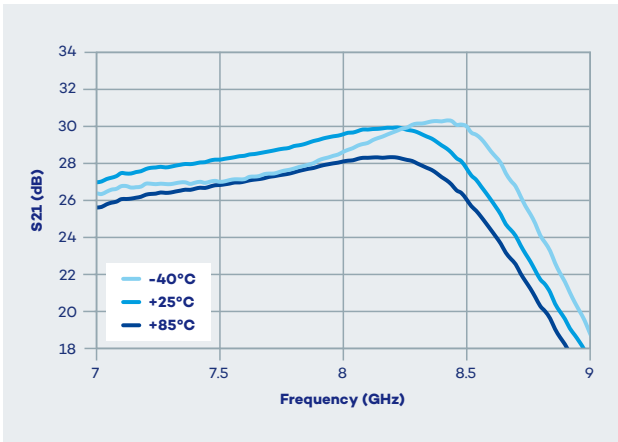
Operation of this device above any of these parameters may cause permanent damage.

• **Typical Performance**
(Small signal / Board Measurement)

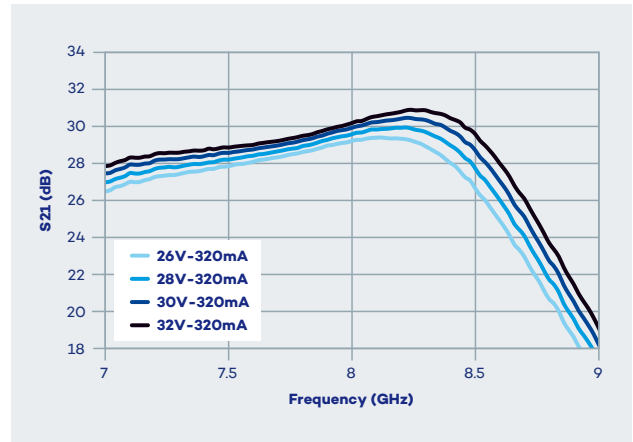
Test conditions: unless otherwise specified

- Reference plane: connector access
- $V_D = +28V$
- $I_{DQ} = 320mA$ ($V_G = -2.4V$ Typ.)
- $P_{in} = -20dBm$

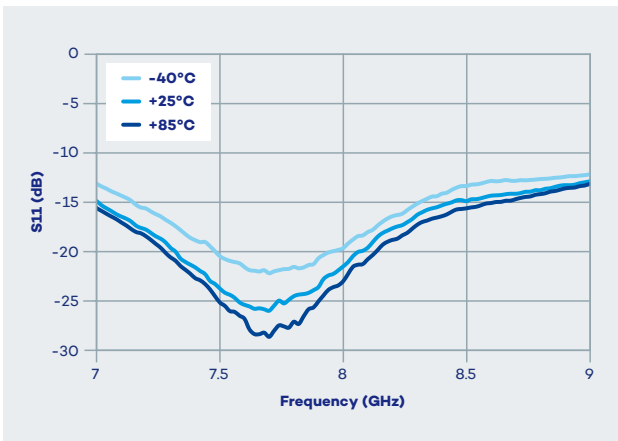
Gain vs Frequency vs Temperature



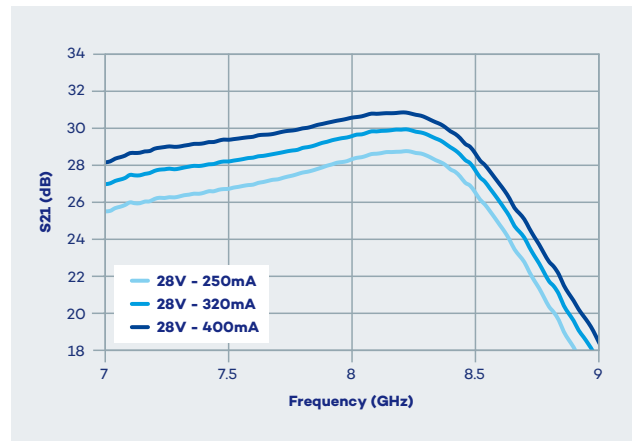
Gain vs Frequency vs V_D



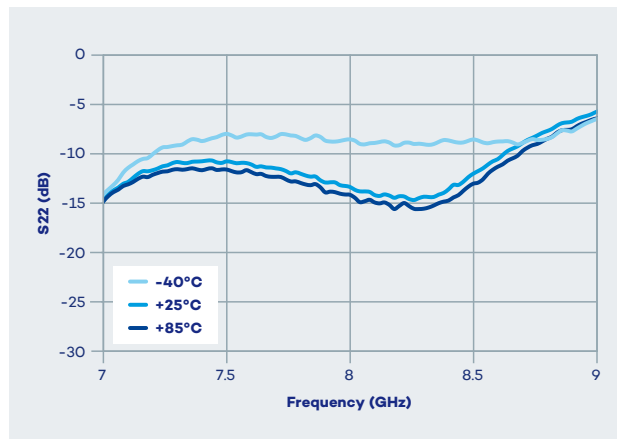
Input Return Loss vs Frequency vs Temperature



Gain vs Frequency vs I_{DQ}



Output Return Loss vs Frequency vs Temperature

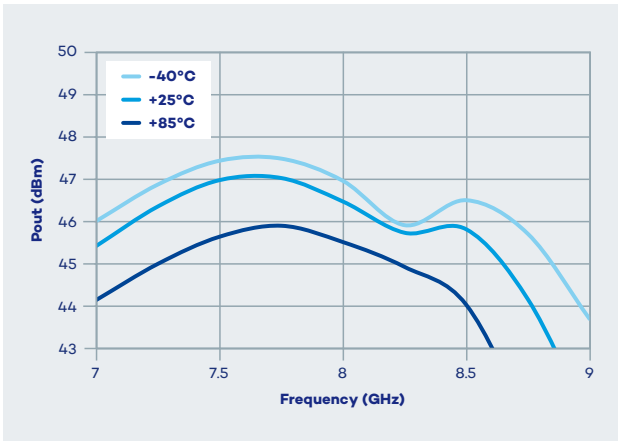


• **Typical Performance**
(Large signal / Board Measurement)

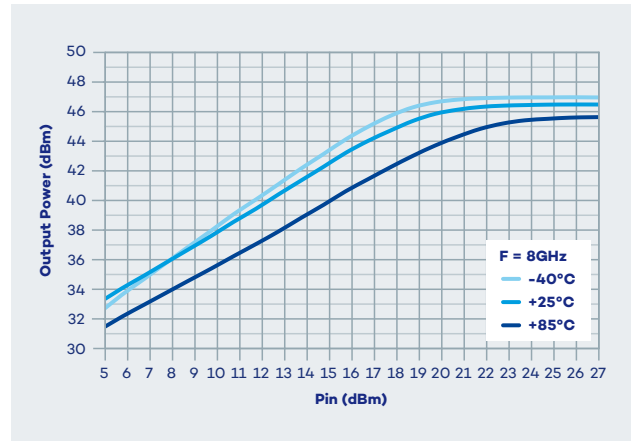
Test conditions: unless otherwise specified

- Reference plane: die access
- $V_D = +28V$
- $I_{BQ} = 320mA$ ($V_G = -2.4V$ Typ.)
- $P_{in} = +25dBm$
- Pulsed mode (pulse width: $30\mu s$, duty cycle: 10%)

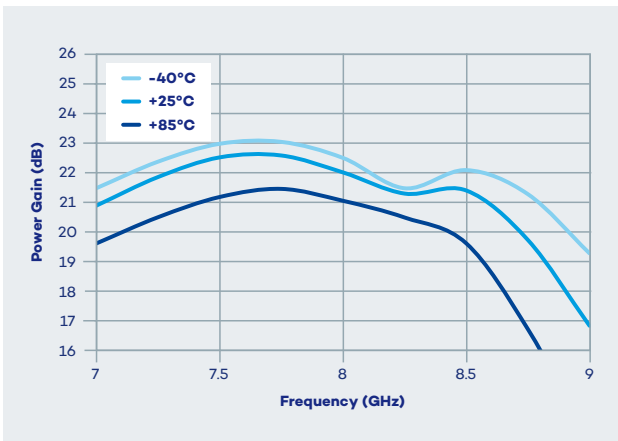
Output Power vs Frequency vs Temperature



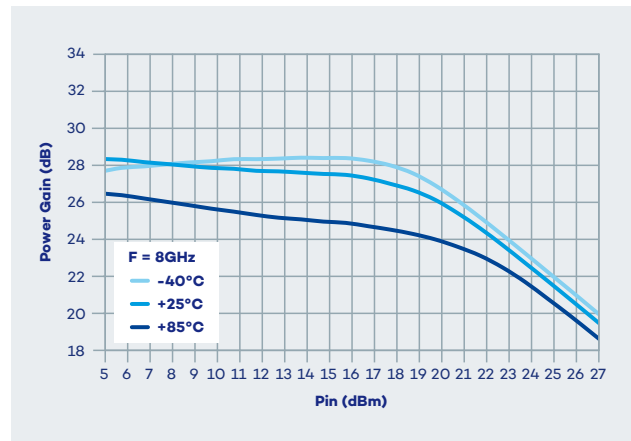
Output Power vs Input Power vs Temperature



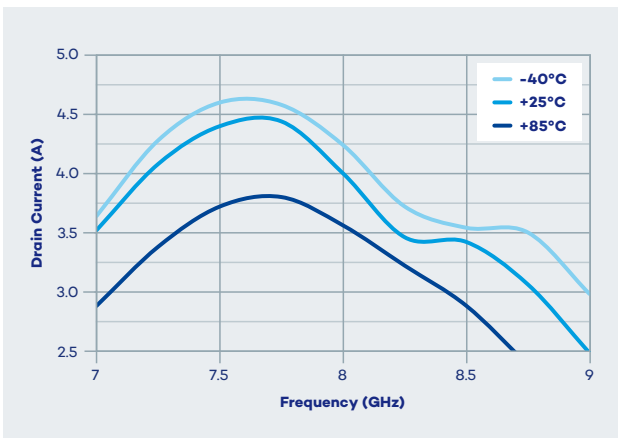
Power Gain vs Frequency vs Temperature



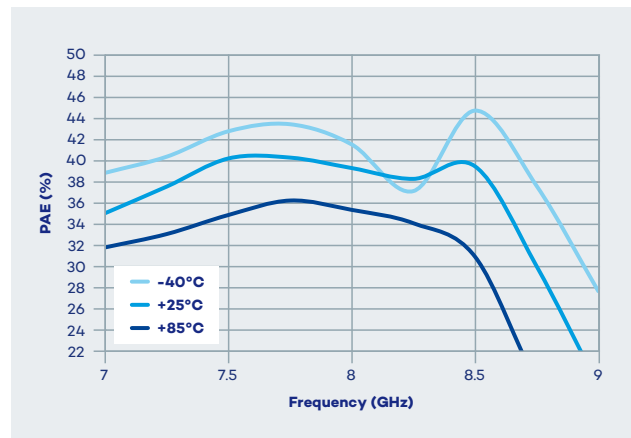
Gain vs Input Power vs Temperature



Drain Current vs Frequency vs Temperature



PAE vs Frequency vs Temperature

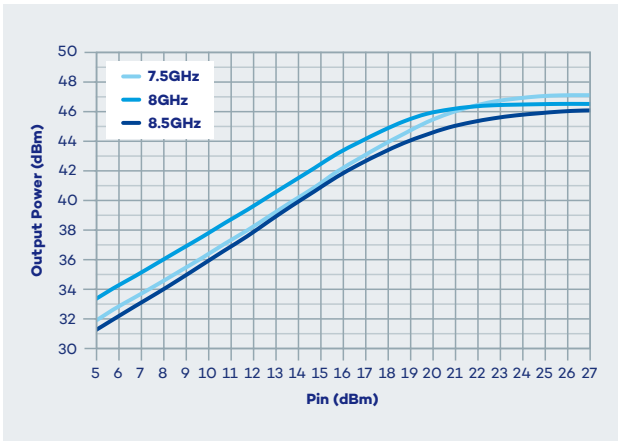


• **Typical Performance**
(Large signal / Board Measurement)

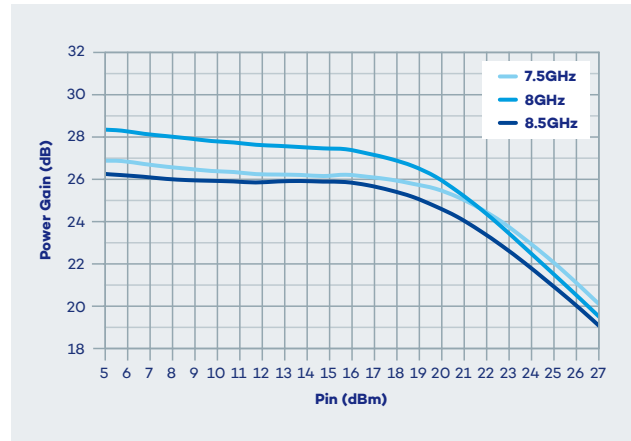
Test conditions: unless otherwise specified

- Reference plane: die access
- $V_D = +28V$
- $I_{DQ} = 320mA$ ($V_G = -2.4V$ Typ.)
- $T_{amb} = +25^\circ C$
- Pulsed mode (pulse width: 30 μs , duty cycle: 10%)

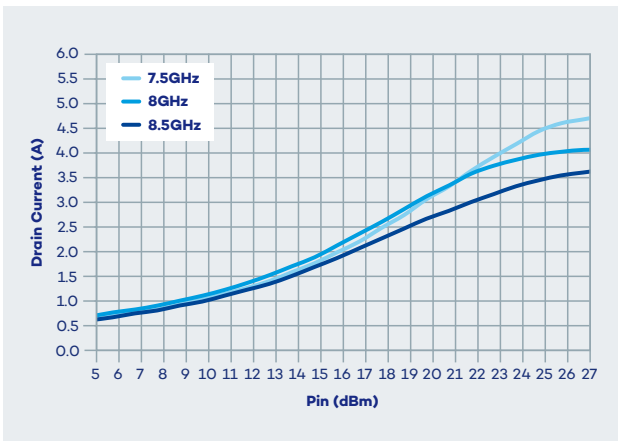
Output Power vs Input Power vs Frequency



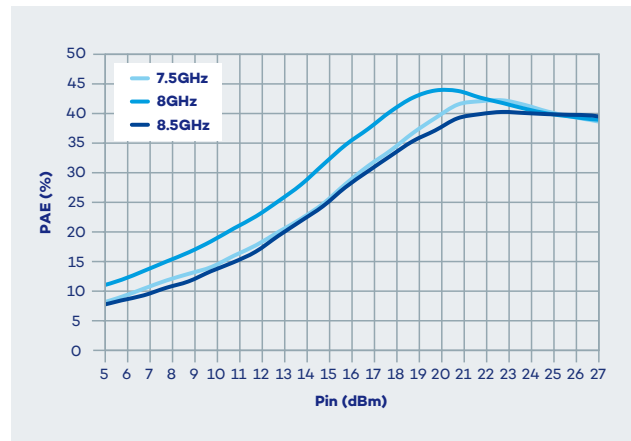
Gain vs Input Power vs Frequency



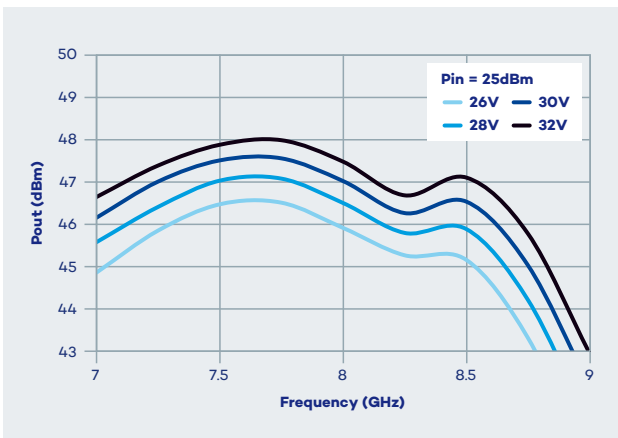
Drain Current vs Input Power vs Frequency



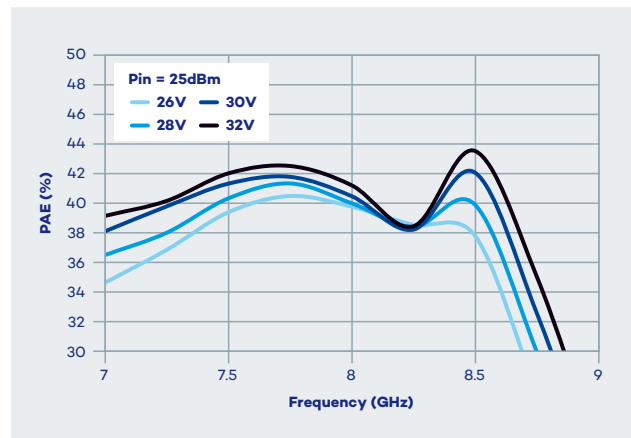
PAE vs Input Power vs Frequency



Output Power vs Frequency vs V_D



PAE vs Frequency vs V_D

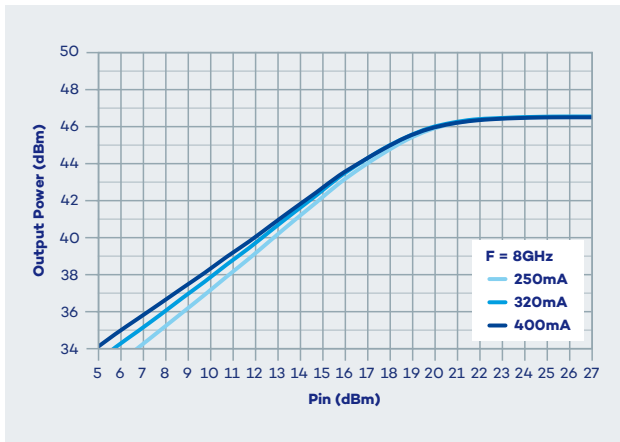


• **Typical Performance**
(Large signal / Board Measurement)

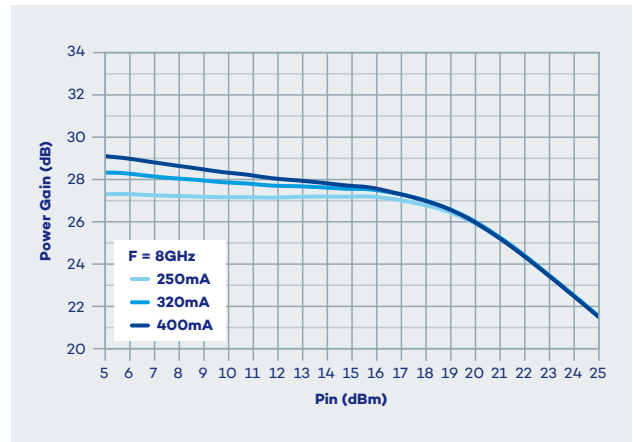
Test conditions: unless otherwise specified

- Reference plane: die access
- $V_D = +28V$
- $T_{amb} = +25^\circ C$
- Pulsed mode (pulse width: 30 μs , duty cycle: 10%)

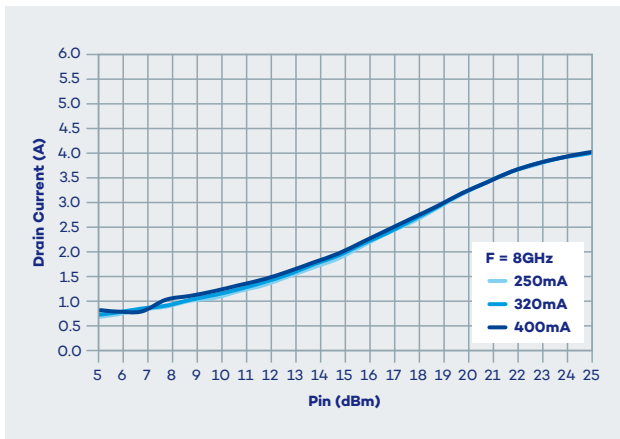
Output Power vs Input Power vs I_{DQ}



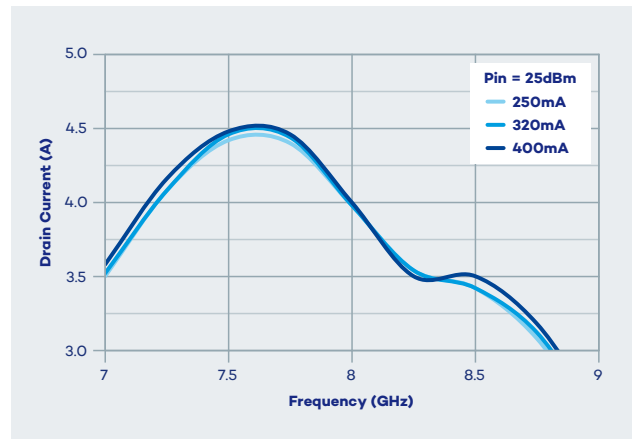
Gain vs Input Power vs I_{DQ}



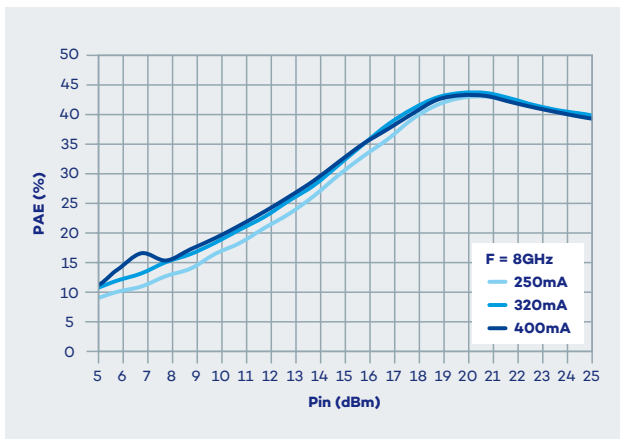
Drain Current vs Input Power vs I_{DQ}



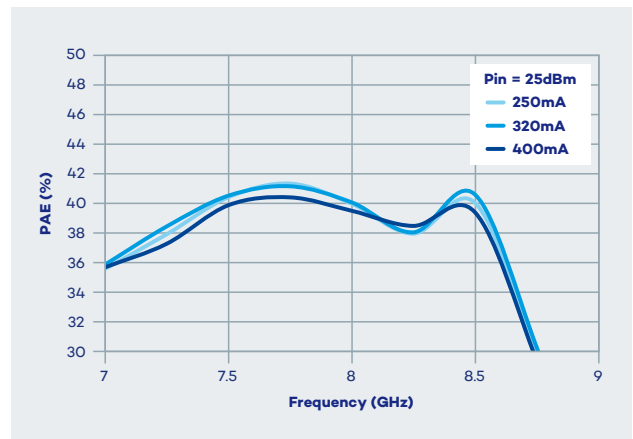
Drain Current vs Frequency vs I_{DQ}



PAE vs Input Power vs I_{DQ}

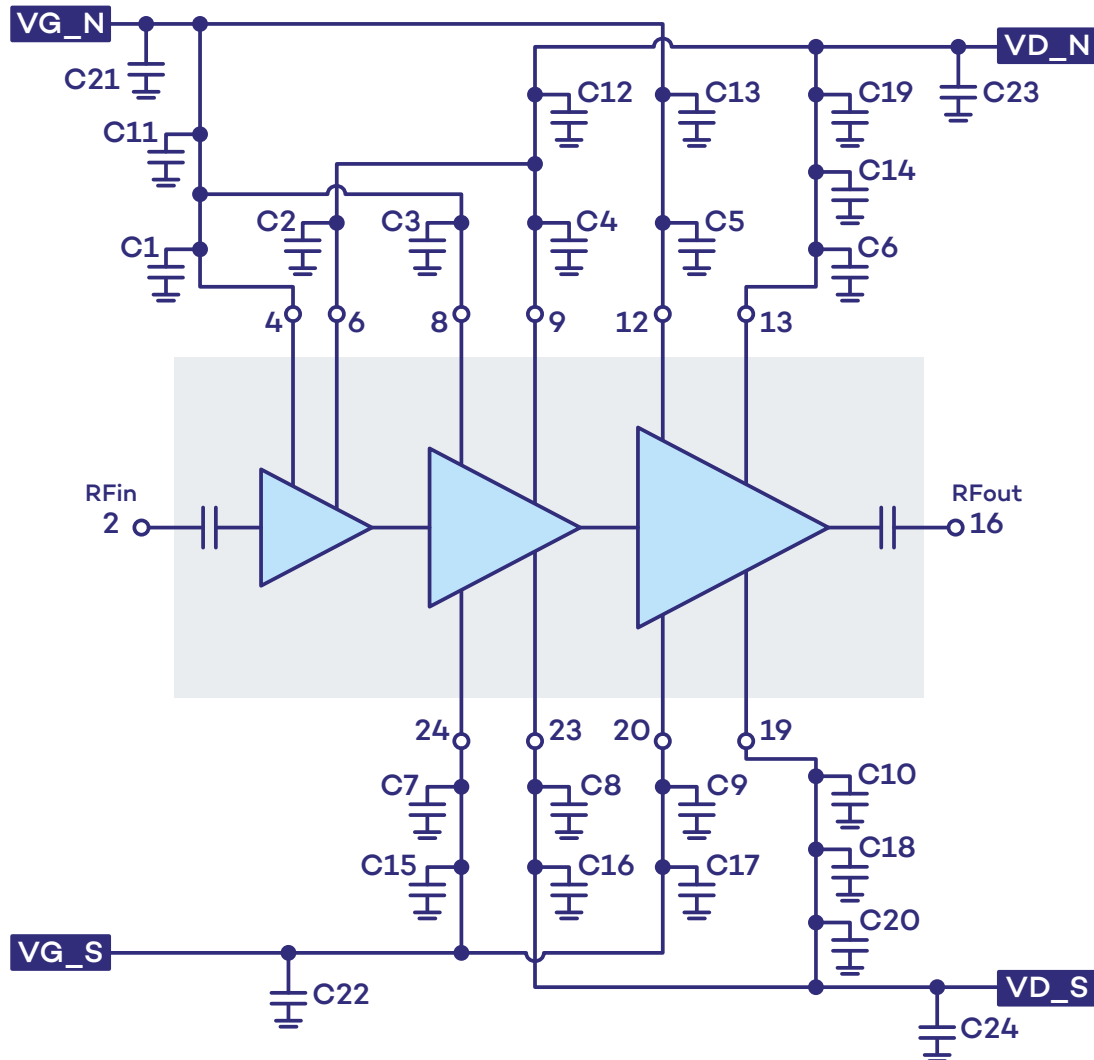


PAE vs Frequency vs I_{DQ}



• **Application circuit**

- C1 to C10 = 100pF
- C11 to C18 = 1nF
- C19, C20 = 10nF
- C21, C22 = 1μF
- C23, C24 = 1μF 50V
- C1 to C20 should be MIM capacitors



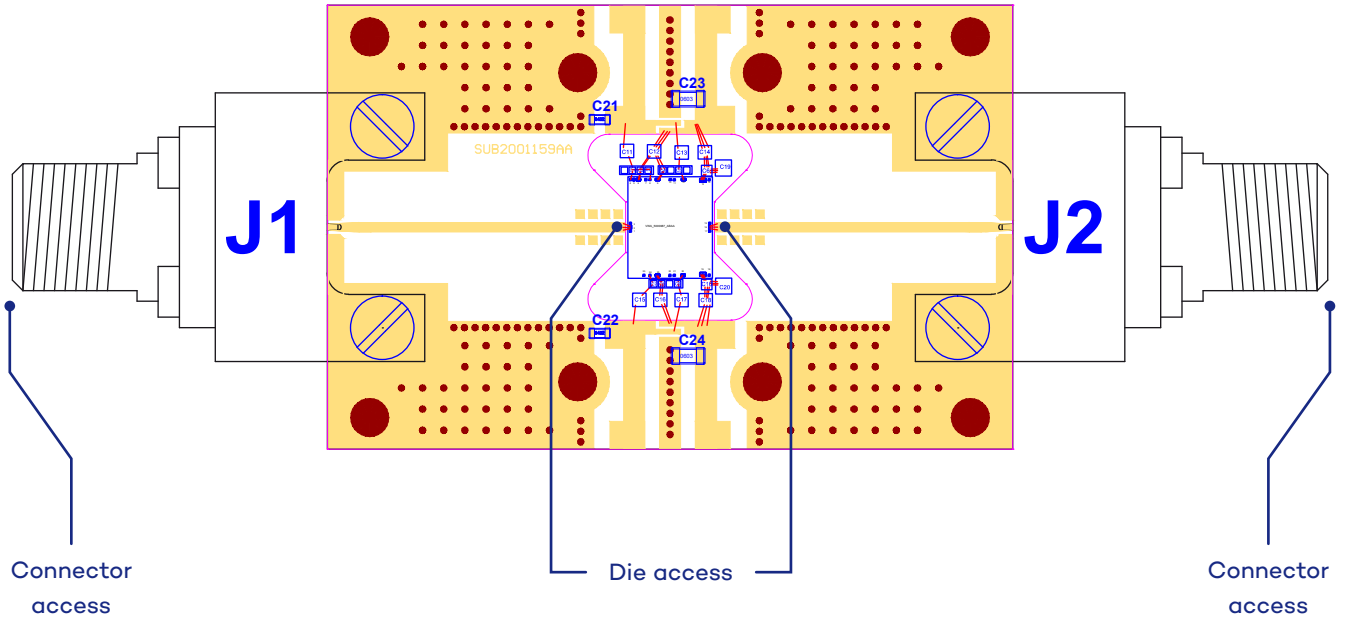
• **Bias-up procedure**

1. Apply $V_G = -3V$
2. Apply $V_D = +28V$
3. Adjust V_G to obtain the specified $I_{DQ} = 320\text{ mA}$ ($V_G = -2.4V$ Typ.)
4. Apply RF signal in pulsed mode

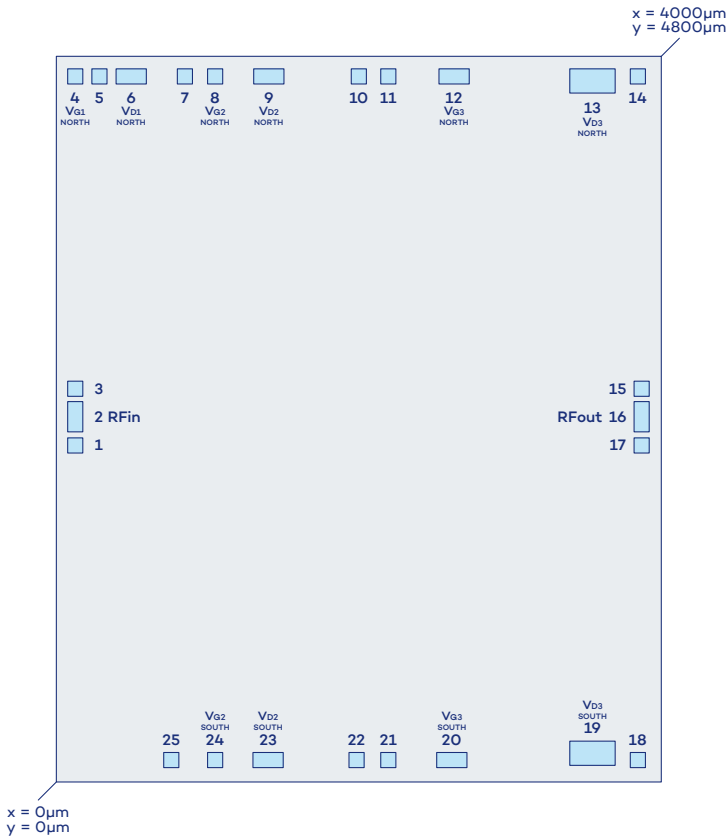
• **Bias-down procedure**

1. Turn off RF signal
2. Reduce $V_G = -3V$
3. Apply $V_D = 0V$
4. Turn off power supply

- Evaluation Board (EVB) Layout Assembly



• Die Layout & Pin Out



- Die size = 4000µm x 4800µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	125	2225	100 x 100	Gnd	
2	125	2415	100 x 200	RFin	RF Input
3	125	2600	100 x 100	Gnd	
4	125	4665	100 x 100	V _{G1} _NORTH	Gate Bias
5	285	4665	100 x 100	Gnd	
6	495	4665	200 x 100	V _{D1} _NORTH	Drain Bias
7	850	4665	100 x 100	Gnd	
8	1050	4665	100 x 100	V _{G2} _NORTH	Gate Bias
9	1405	4665	200 x 100	V _{D2} _NORTH	Drain Bias
10	2000	4665	100 x 100	Gnd	
11	2195	4665	100 x 100	Gnd	
12	2630	4665	200 x 100	V _{G3} _NORTH	Gate Bias
13	3545	4635	300 x 160	V _{D3} _NORTH	Drain Bias
14	3845	4665	100 x 100	Gnd	
15	3870	2600	100 x 100	Gnd	
16	3870	2415	100 x 200	RFout	RF Output
17	3870	2225	100 x 100	Gnd	
18	3845	145	100 x 100	Gnd	
19	3545	190	300 x 160	V _{D3} _SOUTH	Drain Bias
20	2615	145	200 x 100	V _{G3} _SOUTH	Gate Bias
21	2195	145	100 x 100	Gnd	
22	1985	145	100 x 100	Gnd	
23	1400	145	200 x 100	V _{D2} _SOUTH	Drain Bias
24	1050	145	100 x 100	V _{G2} _SOUTH	Gate Bias
25	760	145	100 x 100	Gnd	

- Die bottom must be connected to ground (RF and DC)

• Ordering information

Product Code	Parameter
VM087D	7.5 to 8.5GHz - 40W GaN/SiC Power Amplifier in die form

• Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurements files (S2P)

• Product Compliance Information

Solderability

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivity Rating

Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114



RoHS-Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

• Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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