8.5 to 10.5GHz / 20dB / 40dBm GaN/SiC Transceiver chip

General Description

The **VWA5000091AA** is a transceiver chip designed on a 0.25µm HEMT (High Electron Mobility Transistor) process on GaN/SiC technology.

The device covers the 8.5 to 10.5GHz bandwidth. It is including a switch used to commute the receiver or the transmitter channel to the common access. The transmitter channel is composed by a 3 stages power amplifier and is capable to deliver more than +40dBm of output power at the common access. The receiver channel is composed by a low noise amplifier and can be completed by a second embeedded low noise amplifier and inter-stage attenuators, according to the chosen cabling configuration.

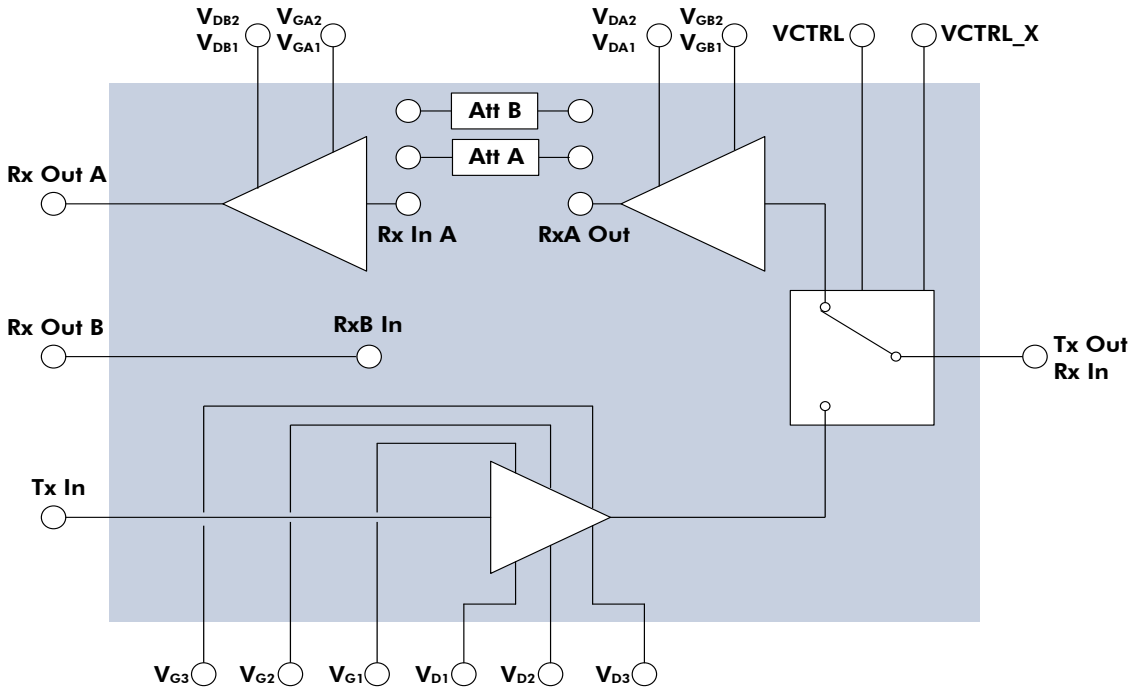
Features

- Transceiver HEMT GaN/SiC MMIC.
- Wide band: 8.5 to 10.5GHz.
- 50ΩRF AC coupled TX Input, RX Output, Common.
- Tx Output Psat >+40dBm
- Tx Gain >+20dB
- Rx Gain >+20dB
- Rx Noise Figure <4dB
- Chip size: 5 x 4 x 0.1 (mm)

Applications

- T/R Module
- Radar / ECM / ECCM
- Test and measurement
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Electrical Specifications

Test conditions unless otherwise noted:

- Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8.5		10.5	GHz
BW	Operating Bandwidth		2000		MHz

Tx Mode with input signal in pulsed mode (width : 10µs, Duty cycle : 10%)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Tx Gain	Tx Small signal gain		23		dB
Tx S11	Tx Input return loss		-10		dB
Tx S22	Tx Output return loss		-8		dB
Tx Pout	Tx Output power		41		dBm
Tx PAE	Tx Associated Power Added Efficiency		30		%
Tx I_D	Tx Associated Drain current			2.5	A
Tx V_D	Tx Drain voltage		28		V
Tx P1dB	Tx P1dB compression		40		dBm

Rx Mode (Constant Wave)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Rx Gain A	Rx Small signal gain option A		18		dB
Rx Gain B	Rx Small signal gain option B		34		dB
Rx NF	Rx Noise Figure			5	dB
Rx S11	Rx Input return loss		-10	-5	dB
Rx S22	Rx Output return loss		-14		dB
Rx I_{DA}	Rx Associated Drain current option A		80		mA
Rx V_{DA}	Rx Drain voltage option A		18		V
Rx I_{DB}	Rx Associated Drain current option B		160		mA
Rx V_{DB}	Rx Drain voltage option B		18		V

Recommended Operating Conditions

Symbol	Parameter	Values	Unit
Tx V_{D1}_V_{D2}_V_{D3}	Tx Drain voltage	28	V
Tx I_{DQ} (D1,D2, D3)	Tx Drain quiescent current	90	mA
Tx V_{G1}_V_{G2}_V_{G3}	Tx Gate voltage	-2.4(typ)	V
Tx V_{CTRL_X}	Tx Complementary Swicth control	-40	V
Tx V_{CTRL}	Tx Swicth control	0	V
Rx V_{DA1}_V_{DA2}	Rx Drain voltage option A	18	V
Rx V_{GA1}_V_{GA2}	Rx Gate voltage option A	-2	V
Rx I_{DA} (D1A, D2A)	Rx Drain current option A	80	mA
Rx V_D(A1, A2, B1, B2)	Rx Drain voltage option B	18	V
Rx V_G(A1, A2, B1, B2)	Rx Gate voltage option B	-2	V
Rx I_D(A1, A2, B1, B2)	Rx Drain current option B	160	mA
Rx V_{CTRL_X}	Rx Complementary Swicth control	0	V
Rx V_{CTRL}	Rx Swicth control	-40	V

Absolute Maximum Ratings

Symbol	Parameter	Values	Unit
Tx V_{D1}_V_{D2}_V_{D3}	Tx Drain voltage	35	V
Tx I_{DQ} (D1,D2, D3)	Tx Drain quiescent current	3	A
Tx V_{G1}_V_{G2}_V_{G3}	Tx Gate voltage	-10 to -2	V
Tx Pin	Tx maximum peak input power overdrive	28	dBm
Rx Pin	Rx maximum peak input power overdrive	20	dBm
Tj	Junction temperature	225	°C

Operation of this device above any of these parameters may cause permanent damage.

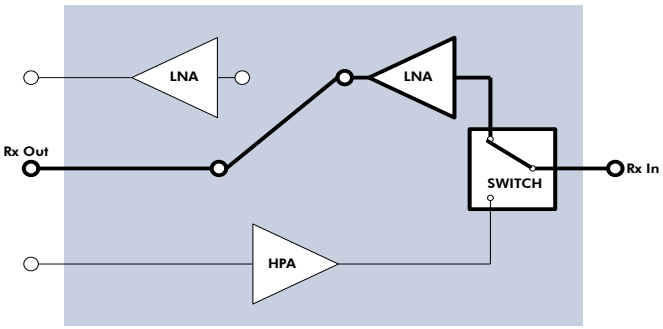
Typical Performance (Test Under Probes)

Test conditions unless otherwise noted:

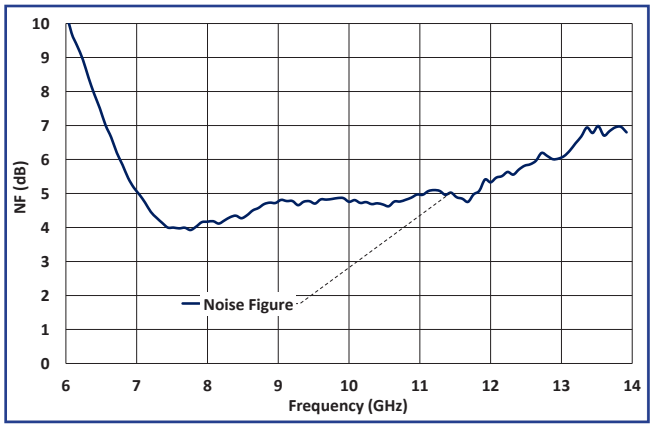
- Tamb.= +25°C
- V_D= +18V
- V_G= -2V
- I_{DQ}= 80mA

One LNA + switch

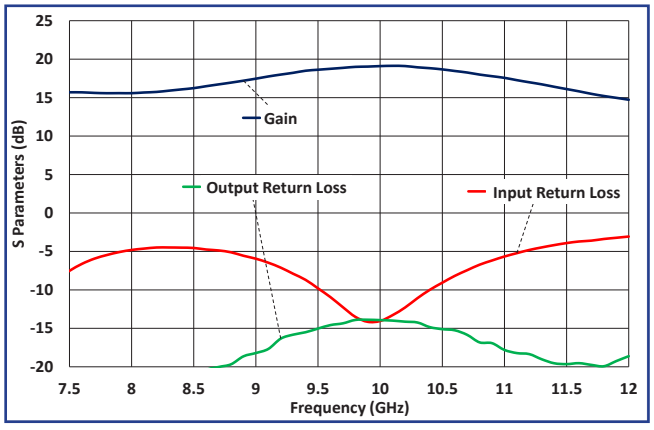
Synoptic in Rx mode



Noise Figure

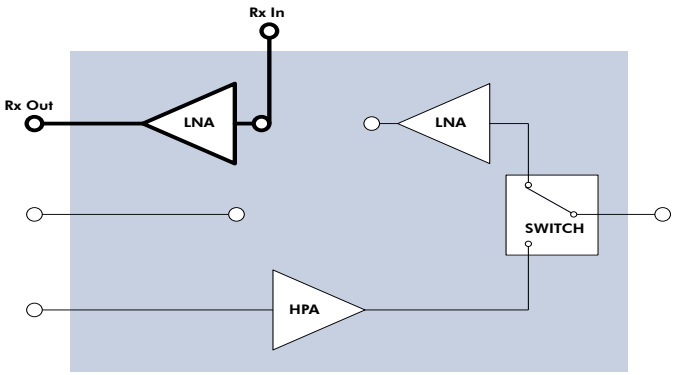


S parameters

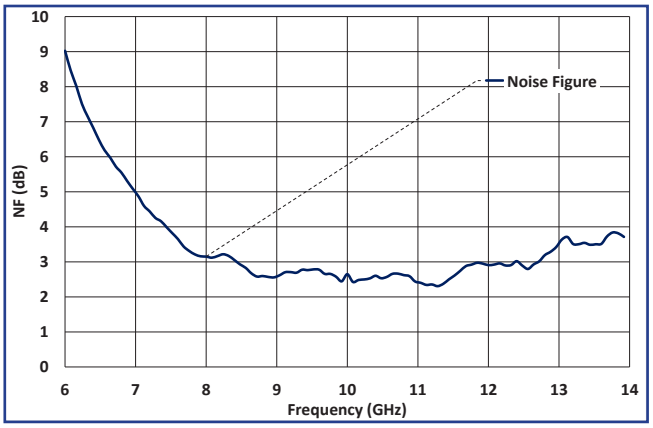


One LNA

Synoptic in Rx mode



Noise Figure



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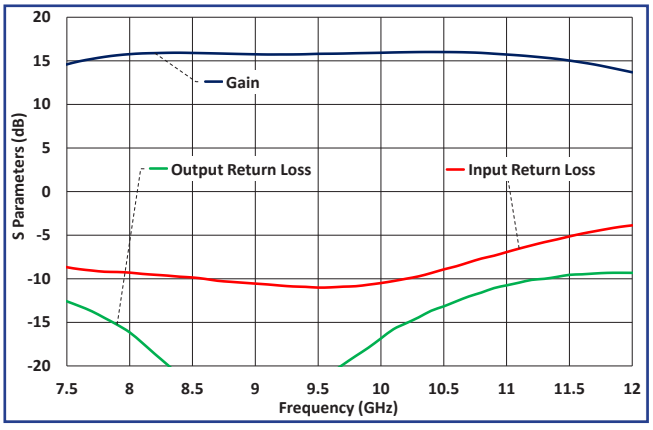


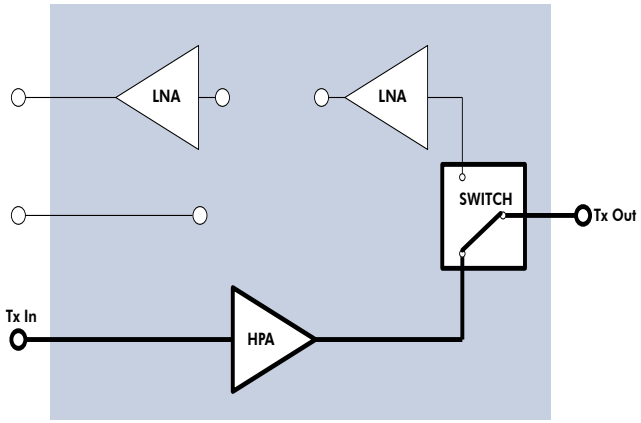
Typical Performance (Test Under Probes)

Test conditions unless otherwise noted:

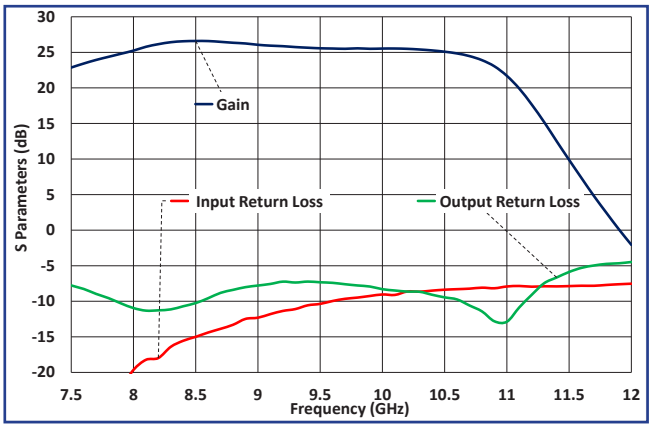
- Tamb.= +25°C
- V_D= +28V
- Switch control voltage= -40V
- V_G= -2.3V
- I_{DQ} = 280mA
- Pulsed mode (Pulse width : 100µs, duty cycle:10%)

HPA + switch

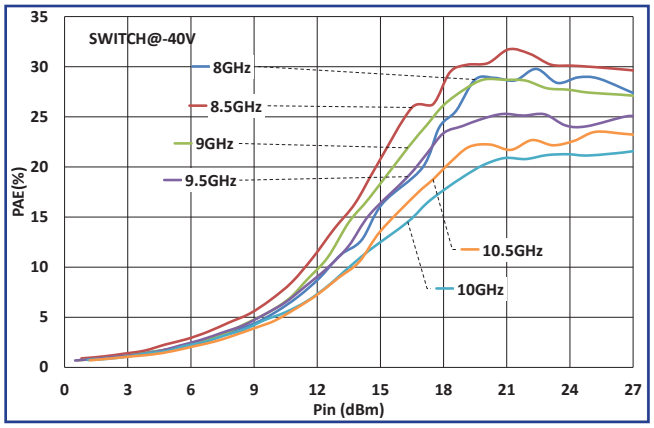
Synoptic with HPA+ switch



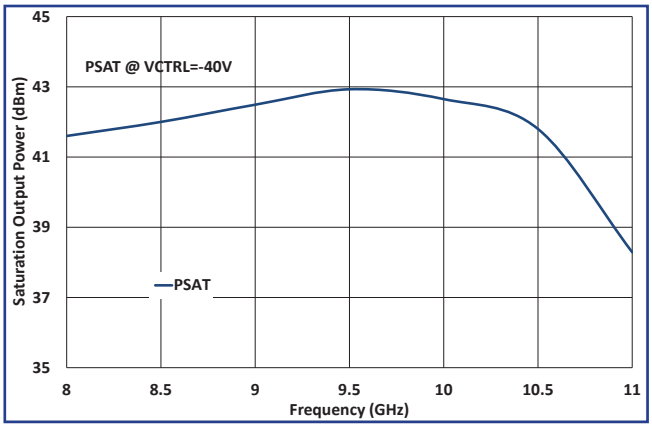
S parameters



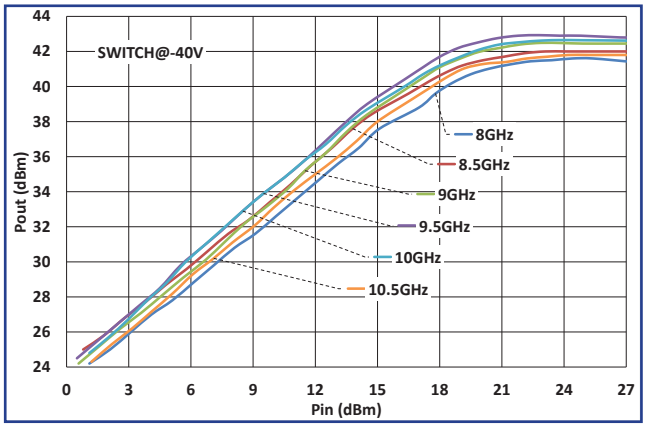
Tx Calculated PAE for V_{CTRL_X} = -40V



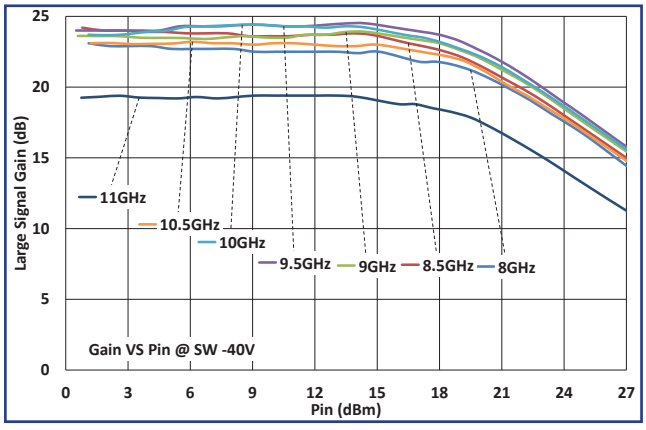
Tx PSAT for V_{CTRL_X} = -40V



Tx Pout VS Pin for V_{CTRL_X} = -40V



Tx large gain for V_{CTRL_X} = -40V

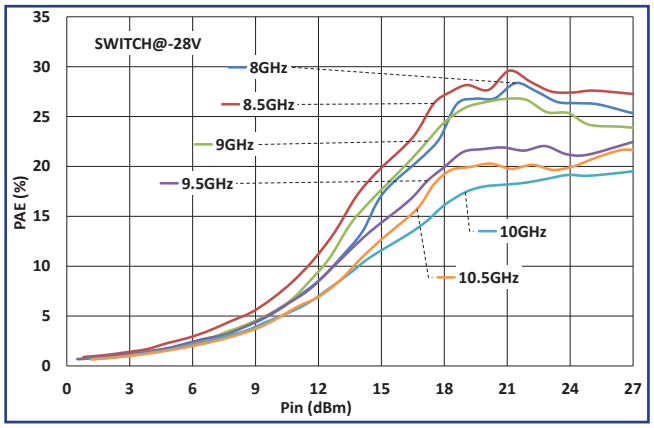


Typical Performance (Test Under Probes)

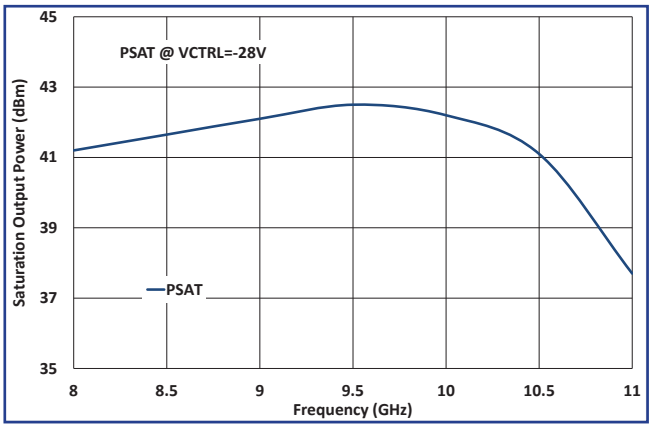
Test conditions unless otherwise noted:

- Tamb.= +25°C
- V_D= +28V
- Switch control voltage= -28V
- V_G= -2.3V
- I_{DQ} = 280mA
- Pulsed mode (Pulse width : 100µs, duty cycle:10%)

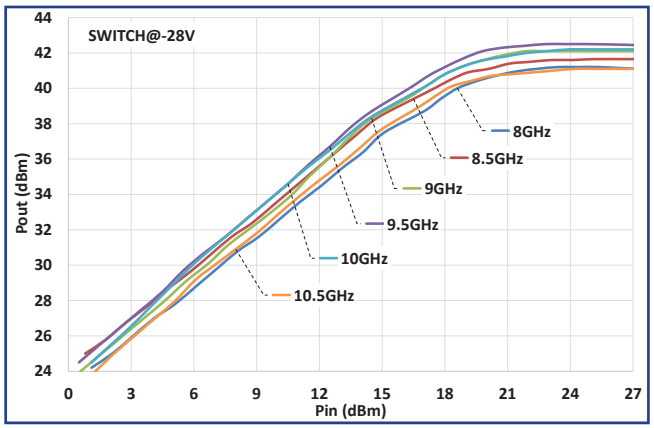
Tx Calculated PAE for V_{CTRL_X} = -28V



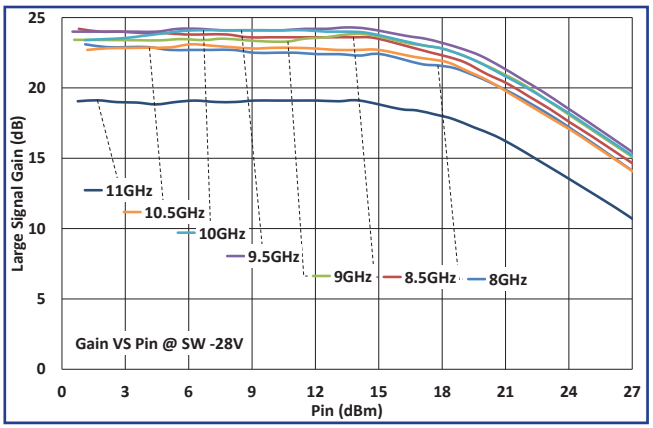
Tx PSAT for V_{CTRL_X} = -28V



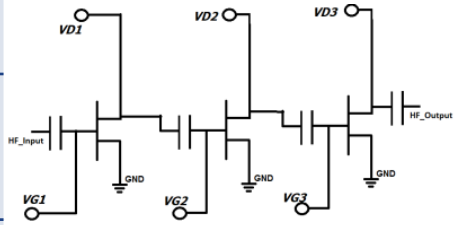
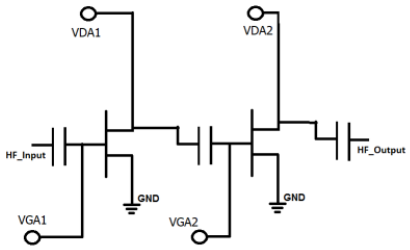
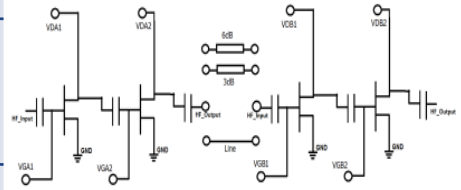
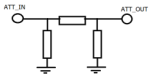
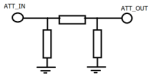
Tx Pout VS Pin for V_{CTRL_X} = -28V



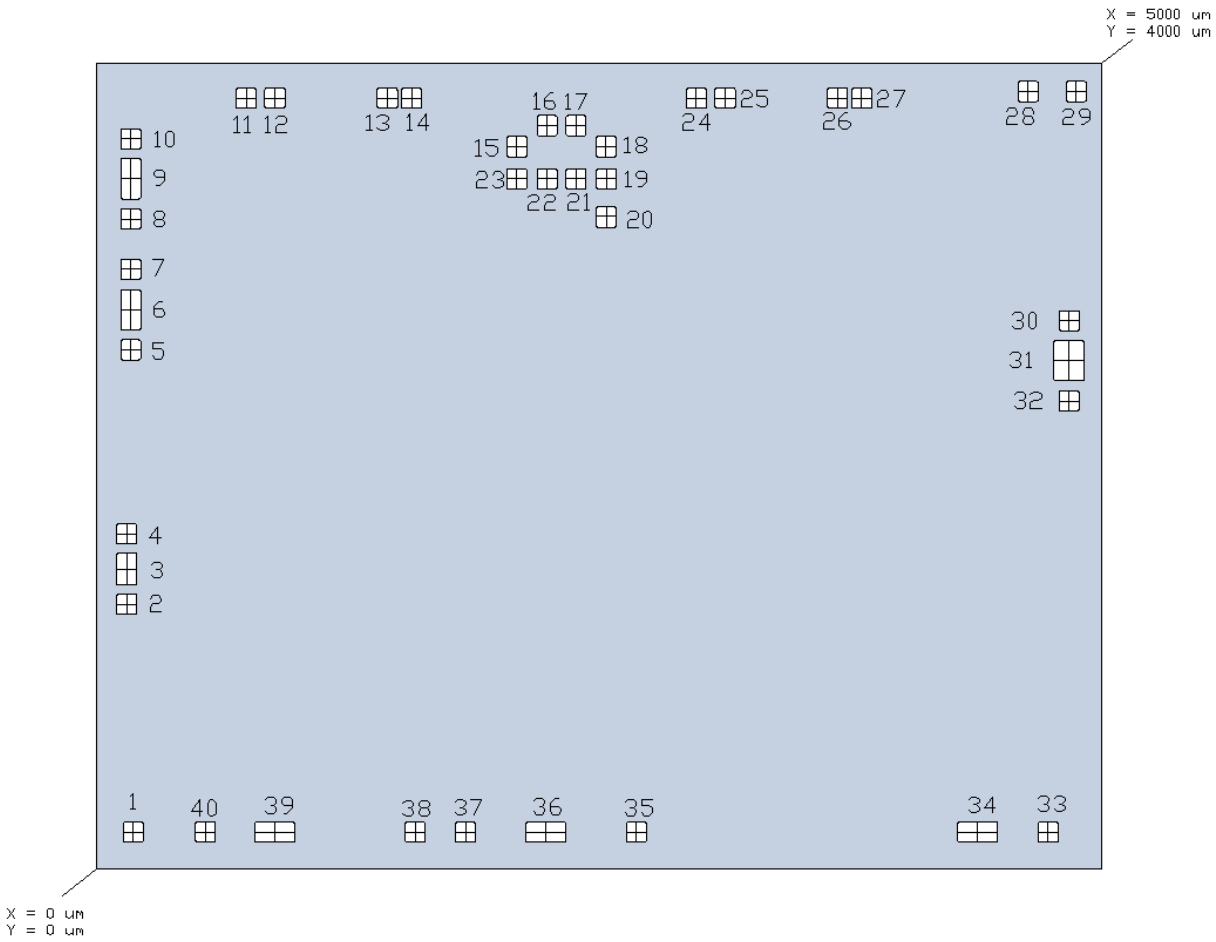
Tx large gain for V_{CTRL_X} = -28V



Access Description

Pin Number	Name	Description	Electrical interface
3	Tx In	TX_HPA Amplifier input, this access is AC coupled and internally matched to 50Ω.	
35, 38, 40	V_{G1} V_{G2} V_{G3}	TX_HPA Gate biasing input accesses. These accesses must be connected to a MIM 100pF, using a small bonding length wire (300µm<L<500µm).	
34, 36 ,39	V_{D1} V_{D2} V_{D3}	TX_HPA Drain biasing input accesses. These accesses must be connected to a MIM 100pF, 50V capacitor using a small bonding length wire (300µm<L<500µm).	
31	Tx Out	TX_Output, this access is AC coupled and internally matched to 50Ω.	
28, 29	V_{CTRL} V_{CTRLX}	VCTRL and VCTRLX are complementary switching control access for TX to RX mode commutation	
31	Rx In	RX_LNA input, this access is AC coupled and internally matched to 50Ω.	
12, 14, 25, 27	V_{GA2} V_{GA1}	RX_LNA Gate biasing input accesses. These accesses must be connected to a MIM 100pF using a small bonding length wire (300µm<L<500µm).	
11, 13, 24, 26	V_{DA2} V_{DA1}	RX_LNA Drain biasing input accesses. These accesses must be connected to a MIM 100pF using a small bonding length wire (300µm<L<500µm).	
6	Rx Out A	2 stages RX_LNA output, this access is AC coupled and internally matched to 50Ω. It is necessary to connect the pads 19 and 20 together using bonding wire connection.	
31	Rx In	HF Amplifier input, this access is AC coupled and internally matched to 50Ω.	
25, 27	V_{GA2}, V_{GA1} V_{GB1}, V_{GB2}	Gate biasing input accesses. These accesses must be connected to a MIM 100pF, using a small bonding length wire (300µm<L<500µm).	
24, 26	V_{DA2}, V_{DA1} V_{DB1}, V_{DB2}	Drain biasing input accesses. These accesses must be connected to a MIM 100pF, 50V capacitor using a small bonding length wire (300µm<L<500µm).	
9	Rx Out B	HF Amplifier output, this access is AC coupled and internally matched to 50Ω. It is necessary to connect the pads 19 and 21 together and 22 to 23 together by using bonding wire connection.	
15, 16	Att1 Access	Embedded 3dB attenuator	
17, 18	Att2 Access	Embedded 6dB attenuator	
Die Bttom	GND	Die must be connected to HF and DC Ground	

Die Layout



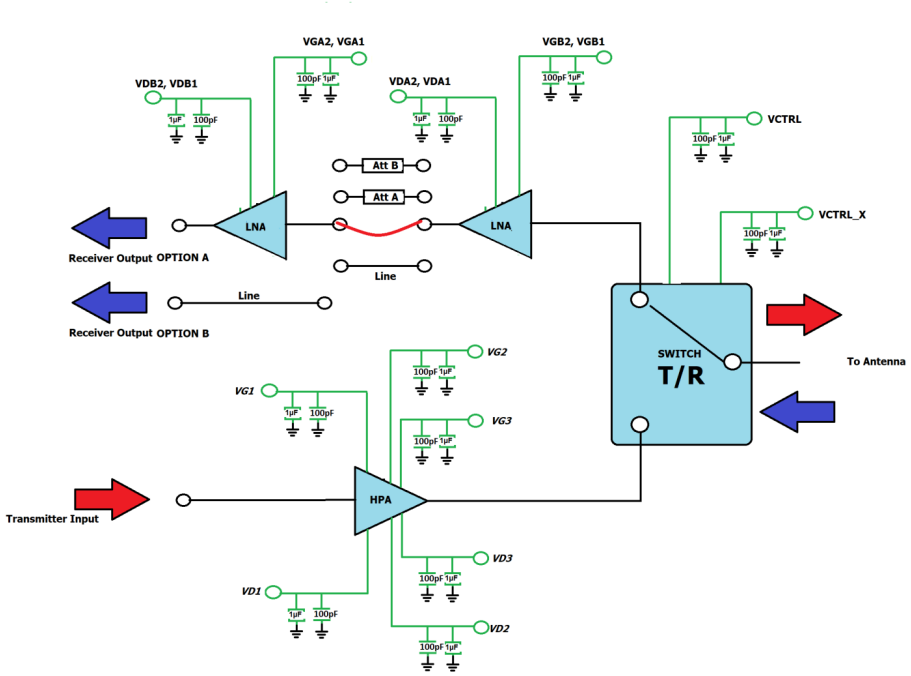
Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

Pinout and Bonding Pad Coordinates

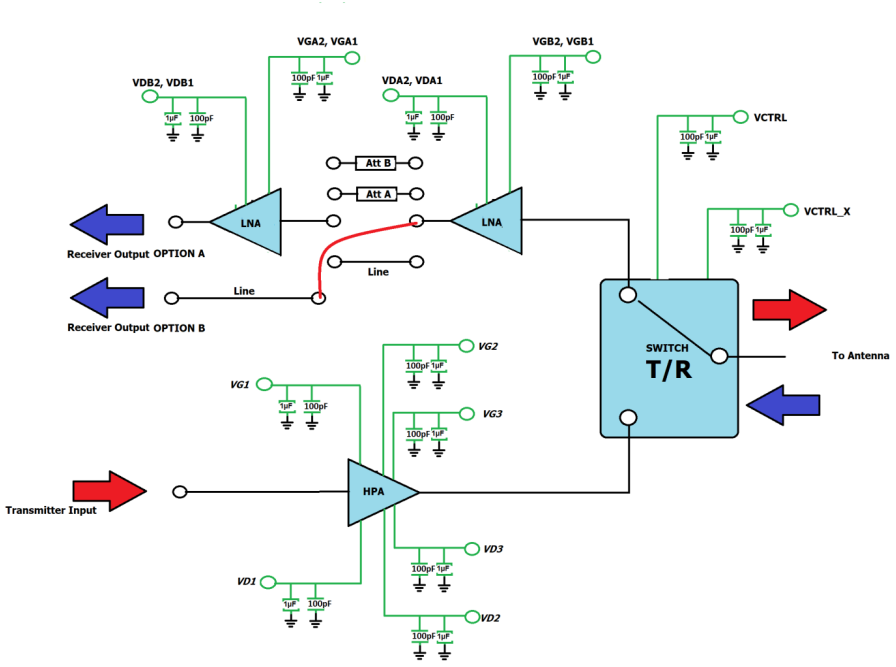
Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	180	180	100*100	GND
2	150	1310	100*100	GND
3	150	1480	160*100	Tx_In
4	150	1660	100*100	GND
5	170	2580	100*100	GND
6	170	2780	200*100	Rx_Out_A
7	170	2980	100*100	GND
8	170	3230	100*100	GND
9	170	3430	200*100	Rx_Out_B
10	170	3630	100*100	GND
11	750	3820	100*100	V_{DB2}
12	890	3820	100*100	V_{GB2}
13	1450	3820	100*100	V_{DB1}
14	1560	3820	100*100	V_{GB1}
15	2090	3588	100*100	Att1_In
16	2260	3700	100*100	Att1_Out
17	2380	3700	100*100	Att2_Out
18	2530	3600	100*100	Att2_In
19	2530	3420	100*100	RxA_Out
20	2530	3240	100*100	Rx_Out_A
21	2380	3420	100*100	Line_In
22	2240	3420	100*100	Line_Out
23	2090	3420	100*100	Rxb_In
24	2980	3820	100*100	V_{DA2}
25	3128	3820	100*100	V_{GA2}
26	3680	3820	100*100	V_{DA1}
27	3800	3820	100*100	V_{GA1}
28	4630	3860	100*100	V_{CTRL_X}
29	4870	3860	100*100	V_{CTRL}
30	4840	2720	100*100	GND
31	4840	2520	150*200	Tx_Out/Rx_In
32	4840	2320	100*100	GND
33	4735	180	100*100	GND
34	4385	180	200*100	V_{D3}
35	2685	180	100*100	V_{G3}
36	2235	180	200*100	V_{D2}
37	1835	180	100*100	GND
38	1585	180	100*100	V_{G2}
39	885	180	200*100	V_{D1}
40	541	180	100*100	V_{G1}

Application circuit

a) Typical implementation scheme for otion A



b) Typical implementation scheme for otion B



EXTERNAL DECOUPLING COMPONENT recommendation:
For 100pF capacitors, use MIM single layer capacitors: 100pF, 50V in D15/D20 case. It should be placed as close as possible to the die access.
For 1µF capacitors, use SMD multi-layer capacitors: 1µF small form factor (0402/0603) (50V). It can be deported using low serial inductance link. Depending on the mounting environment, it can be useful to add a serial 5-10Ω resistor to the SMD 1µF capacitor. By the way, the resistance makes it possible to damp the resonance associated with the mounting of the non-ideal elements.

Ordering Information

Product Code	Definition
VWA 5000091 AA	8.5 to 10.5 GHz/20dB/40dBm GaN/SiC transceiver chip

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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