8 to 11GHz / 10W GaAs Power Amplifier

DATA SHEE **VM102D**

General Description

The VM0102D is a High Power Amplifier MMIC operating in the frequency range from 8 GHz to 11GHz.

The device delivers more than +40dBm saturated output power, and provides 24dB of small signal gain from 8GHz to 11GHz. The design has been optimized to provide high efficiency higher than 40% under +8V supply voltage.

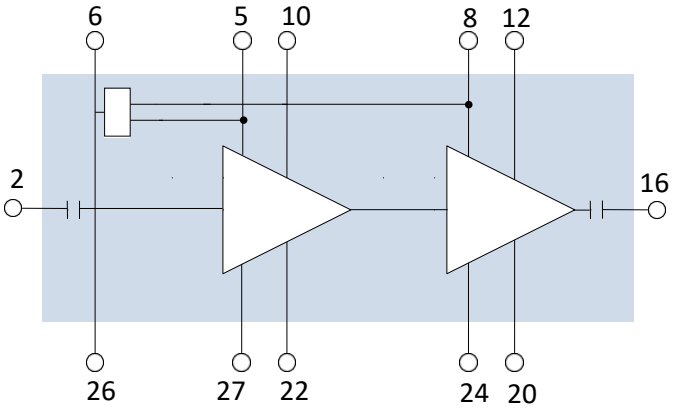
Features

- Frequency band: 8 to11GHz
- Output Power (@ Pin=19dBm) > 40dBm
- PAE (@ Pin=19dBm) > 40%
- P1dB > 39dBm
- Small Signal Gain : 24dB
- 50Ω, AC coupled RF input and output access
- Power supply: I_{DQ}=2.8A; V_D= +8V; V_G= -0.8V
- Chip size: 4.4 x 2.5 x 0.1mm

Applications

- Radar
- Telecommunications
- Test and measurement

Pins Assignment & Functional Block Diagram



Symbol	Pad N°
RF in	2
VSS	6/26
VG1	5/27
VD1	10/22
VG2	8/24
VD2	12/20
RF out	16

Electrical Specifications

Test conditions unless otherwise noted: Post-Layout Simulation

- Tamb.= +25°C
- V_D= V_{D1}= V_{D2}= +8V
- V_G= V_{G1}= V_{G2}= -0.8V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8		11	GHz
BW	Operating Bandwidth		3		GHz
G	Small signal gain		24		dB
Pout	Output power @ Pin= 19 dBm		40		dBm
PAE	Associated Power Added Efficiency @ Pin = 19 dBm		40		%
I_D	Supply current total ($I_D = I_{D1} + I_{D2}$)		3.2		A
V_D	Drain Voltage		8		V
ΔG	Small signal gain flatness		+/- 1.5		dB

Recommended Operating Conditions

- **Post-Layout Simulation**

Symbol	Parameter	Values	Unit
V_D	Drain voltage	8	V
V_G	Gate voltage	-0.8	V

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_D	Drain voltage without RF input		8.5	V
V_G	Direct gate bias voltage	-3	0	V
V_{SS}	Gate bias voltage	-6	-4	V
I_D	Drain bias current ($I_D = I_{D1} + I_{D2}$)		4	A
Pin max	RF input power (peak)		+25	dBm

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Biasing options

Biasing access voltage values:

Pads name	Description	Voltage (V)	Current (A)
V_{D1}	First stage drain biasing access	8	$I_D = I_{D1} + I_{D2} = 3.5$
V_{D2}	Second stage drain biasing access	8	
V_{G1} ; V_{G2}	First stage and second stage gates direct biasing access	$-1 < V_G < -0.7$	$I_G = I_{G1} + I_{G2} = 0.1$
V_{SS}	First stage and second stage compensated applications dedicated gates biasing access	-5	
Die bottom	DC and RF reference	0	

Gate access:

Depending on the applications environment, the gate of each stage can be biased using one of the three next options:

- Option 1:

Direct gate biasing (each stage individually, use V_{G1} and V_{G2}). This option is dedicated for device characterization period and high level of optimized amplifier functioning point.

- Option 2:

Gate biased using internal circuitry (use V_{SS}). This option is dedicated to a dispersion compensation.

Drain access:

The first stage drain can be biased on one side using pad V_{D1}. The second stage drain must be biased using the two pads V_{D2} north & south.

DC Filtering access:

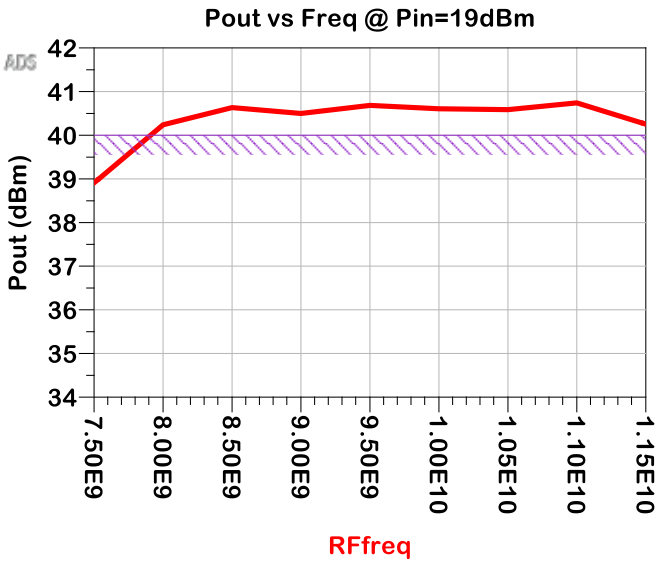
Parallel MIM capacitors must be placed on each used DC pads and on each V_{D1} access, in order to ensure the amplifier performances. Typically, a 100pF value in D20 format can be used. Also additional 10nF single layer capacitor is recommended on each bias connection.

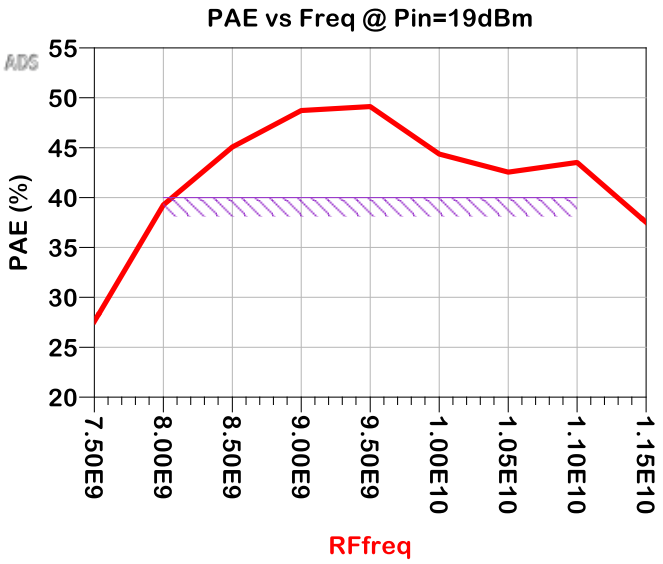
Typical Performance (Post-Layout Simulation)

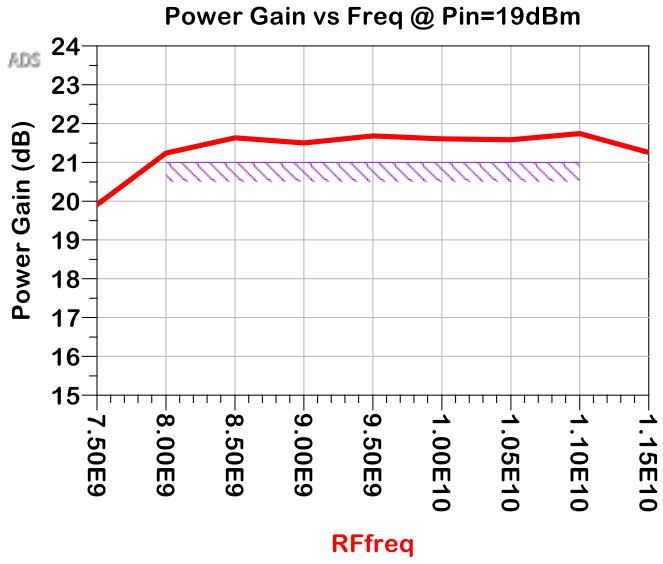
Bias method: Option 1

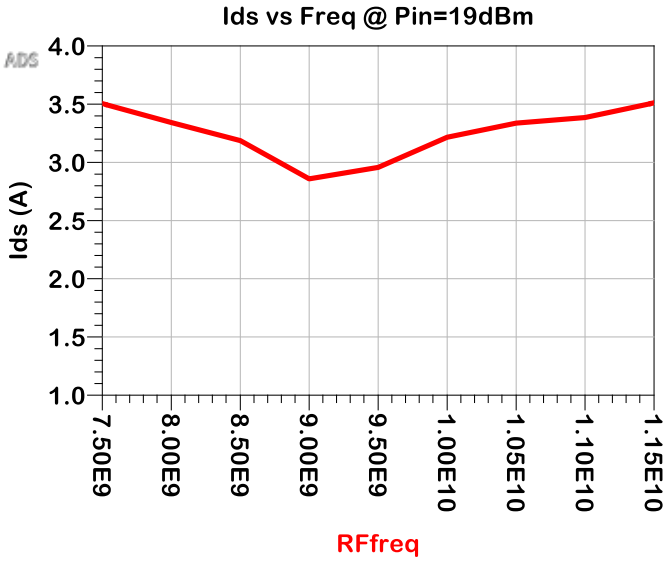
Test conditions: unless otherwise specified

- Tamb.= +25°C
- V_G= V_{G1}= V_{G2}= -0.8V
- V_D= V_{D1}= V_{D2}= +8V
- I_{DQ}= 2.8A







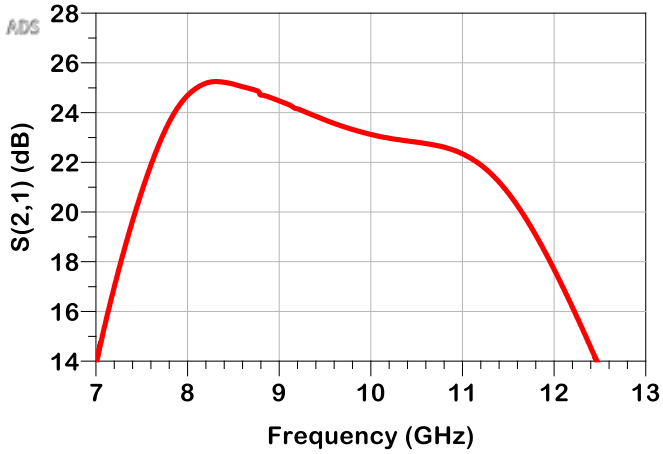


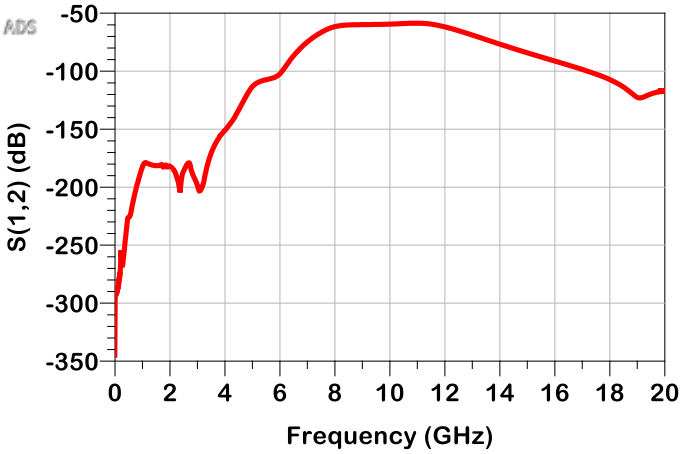
Typical Performance (Post-Layout Simulation)

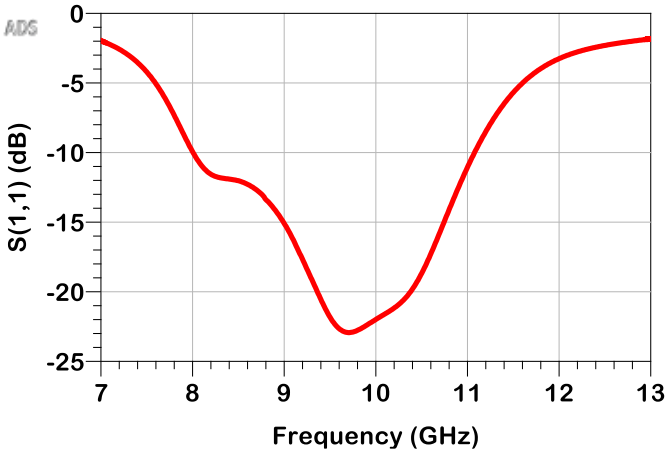
Option 1

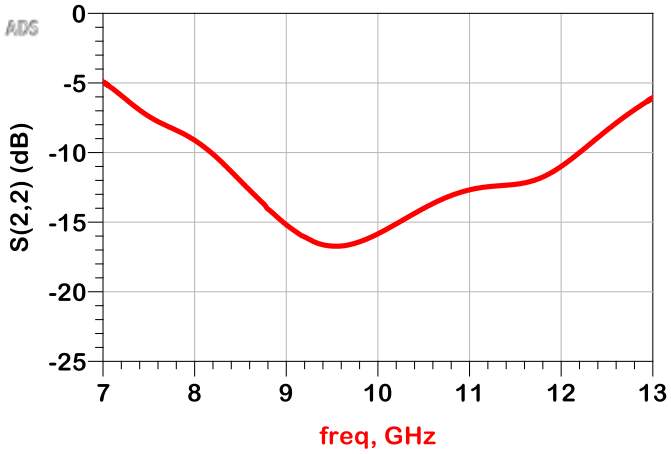
Test conditions: unless otherwise specified, test under probes

- Tamb.= +25°C
- V_G= V_{G1}= V_{G2}= -0.8V
- V_D= V_{D1}= V_{D2}= +8V
- I_{DQ}= 2.8A



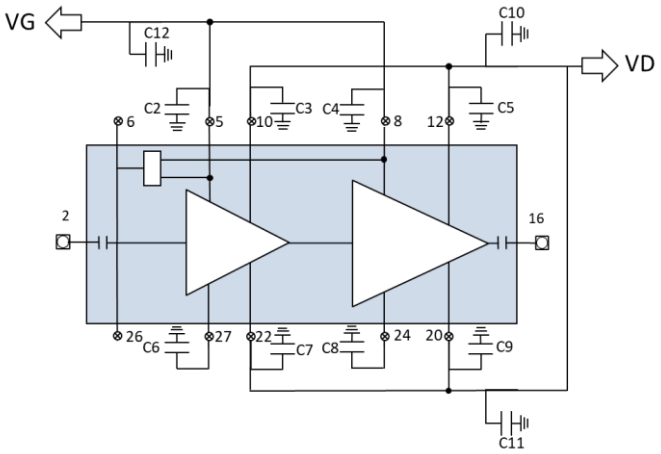




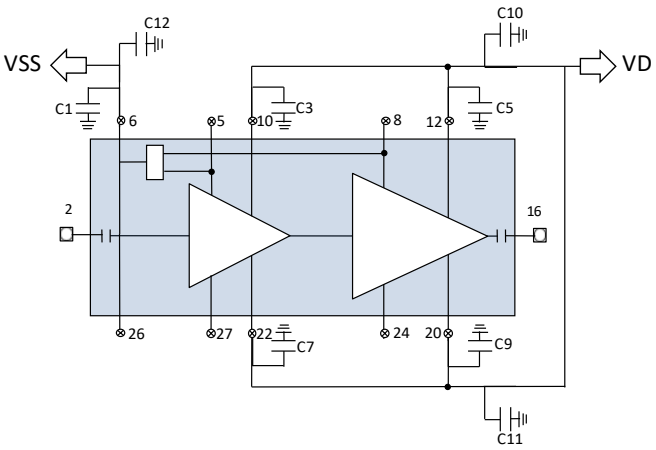


Application Circuit

- C2 to C9 = 100pF should be MIM capacitor
- C10 to C12 = 10nF

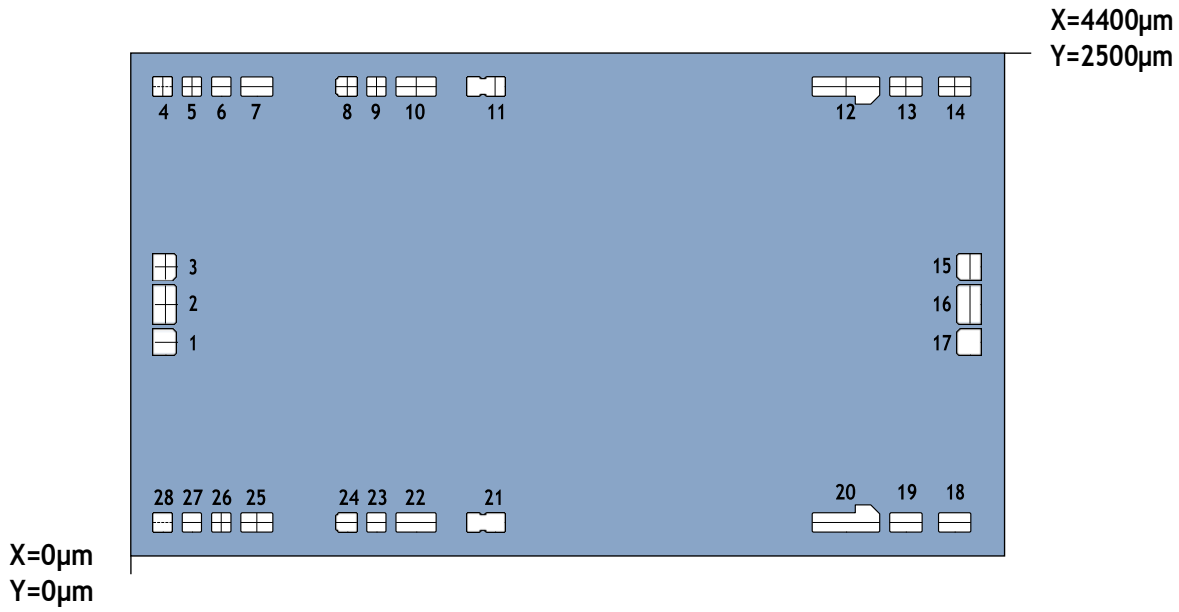


Option1



Option2

Die Layout



Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	125	1050	100x100	GND
2	125	1250	100x200	RF_Input : AC Coupled
3	125	1450	100x100	GND
4	125	2368	100x100	N/A
5	275	2368	100x100	V_{G1}_NORTH
6	425	2368	100x100	V_{SS}_NORTH
7	580	2368	150x100	GND
8	1070	2368	100x100	V_{G2}_NORTH
9	1220	2368	100x100	GND
10	1425	2368	200x100	V_{D1}_NORTH
11	1825	2368	150x100	GND
12	3570	2368	340x100	V_{D2}_NORTH
13	3900	2368	150x100	GND
14	4150	2368	150x100	GND
15	4275	1450	100x100	GND
16	4275	1250	100x200	RF_Output : AC Coupled
17	4275	1050	100x100	GND
18	4150	132	150x100	GND
19	3900	132	150x100	GND
20	3570	132	340x100	V_{D2}_SOUTH
21	1825	132	150x100	GND
22	1425	132	200x100	V_{D1}_SOUTH
23	1220	132	100x100	GND
24	1070	132	100x100	V_{G2}_SOUTH
25	580	132	150x100	GND
26	425	132	100x100	V_{SS}_SOUTH
27	275	132	100x100	V_{G1}_SOUTH
28	125	132	100x100	N/A

- Die thickness = 100µm
- Die bottom must be connected to ground (RF and DC)

Ordering Information

Product Code	Definition
VM0102D	8 to 11 GHz / 10 W

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

Vectrawave SA
5, rue Louis de Broglie
22 300 Lannion
France

www.vectrawave.com
Email sales: contact_sales@vectrawave.com
Tel sales:+33 (0)2 57 63 00 20

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