DC to 18GHz
5 Bit Digital Attenuator

DATA SHEET PRELIMINARY VM103D

General Description

The **VM103D**, is a wide band GaAs MMIC:
- 5-bit attenuator
- Digital control logic

The digital control logic allows for parallel data input, so attenuation value may be changed instantaneously. This broadband Attenuator has an LSB of 0.9dB, and controlled by 5 digital binary inputs, compatible with LVCMOS / TTL levels. This device uses a single -7.5V Bias supply voltage.

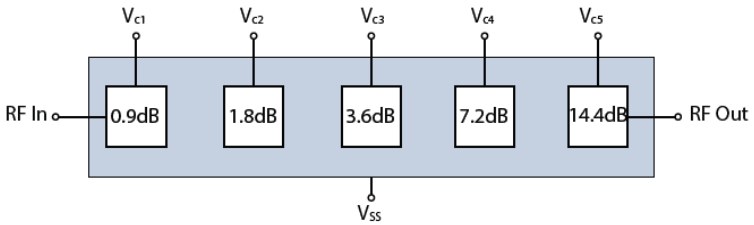
Typical Features

- Operating frequency range: DC to 18GHz
- 5-bit attenuator
- 0.9dB LSB
- 27.9dB Attenuation range
- Digital control (0 / + 3 V)
- 24dBm P1dB input compression
- Parallel data input
- Chip size: 2.38 x 1.55 x 0.1 (mm)

Applications

- Active Antenna
- RF Communication
- RF Front end
- Test and Measurement

Pin Assignment & Functional Block Diagram



Symbol	Pad No
RF In	2
Vc_1	6
Vc_2	7
Vc_3	8
Vc_4	9
Vc_5	10
RF Out	11

Electrical Specifications

Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		18	GHz
LSB	5 Bit Digital Attenuator-Resolution		0.9		dB
A	Attenuation Range		27.9		dB
IL	Insertion Loss @ 10 GHz (Reference state)		4.6		dB
S11	Input Return loss (All states)		-12		dB
S22	Output Return loss (All states)		-12		dB
Input P_{1dB}	Input Power @ 1 dB		24		dBm
RMS A	RMS Attenuation Error		0.5		dB
A Error	Max Attenuation Error		1		dB
RMS P	RMS Phase Error		10		Deg
P Error	Max Phase Error		20		Deg
P Delta	Phase variation @ 10 GHz		15		Deg
ST/SF	Switching speed		TBD		ns
V_{SS}	Supply Voltage		-7.5		VDC
I_{SS}	Supply Current		11		mA
Vci_H	Bit control voltage High	2.5	3	5	V
Vci_L	Bit control voltage Low	0		0.8	V

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{SS}	Supply Voltage	-15		V
Pin	CW RF input power		30	dBm
T process	Soldering temperature		300	°C
Tch	Channel temperature(*)		150	°C
Ta	Operating temperature range	-40	+85	°C
Tstg	Storage temperature range	-55	+150	°C

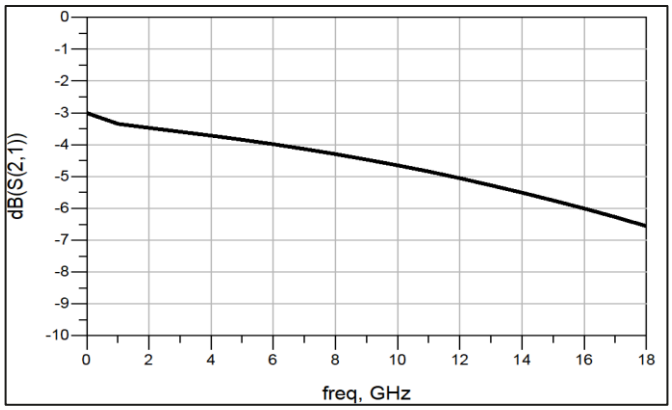
(*)Rth, thermal resistance from junction to backside: TBD
Operation of this device above any of these parameters may cause permanent damage.

Typical Performance (Post-layout Simulations)

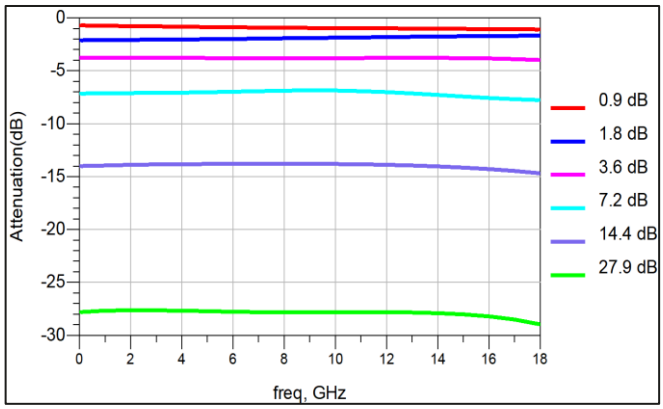
Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

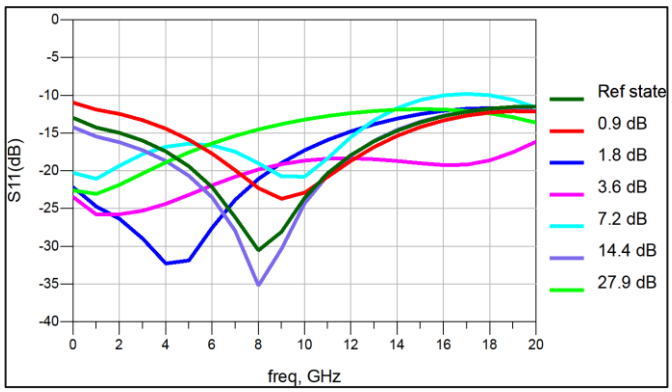
Reference State-insertion loss(dB)



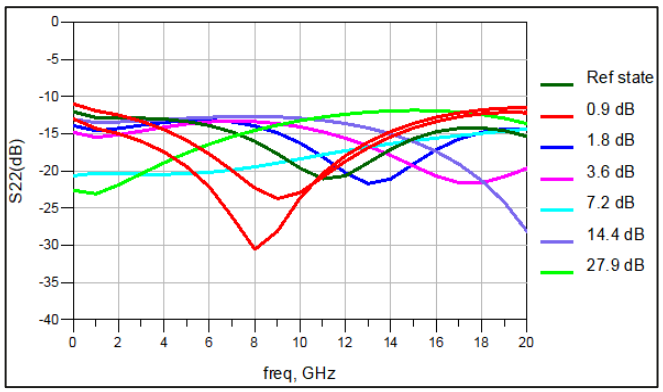
Attenuation level - Major state(dB)



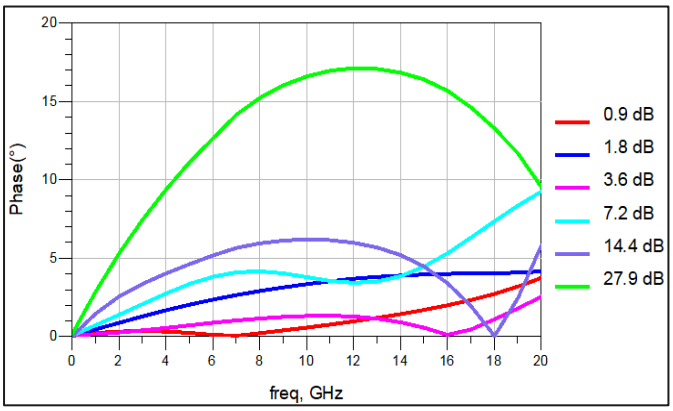
Input Return Loss (dB)



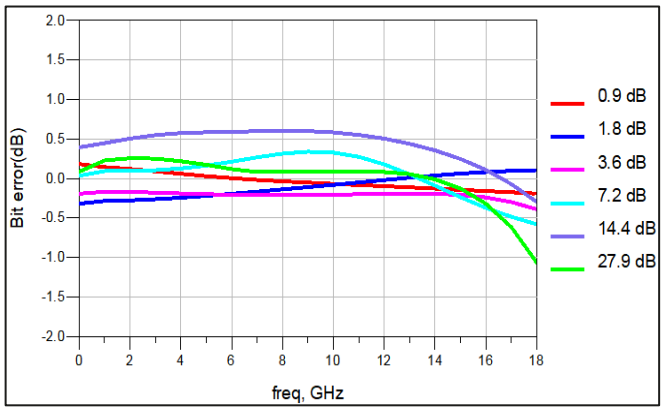
Output Return Loss (dB)



Absolute Relative phase - Major state(deg)



Bit error- Major state(dB)

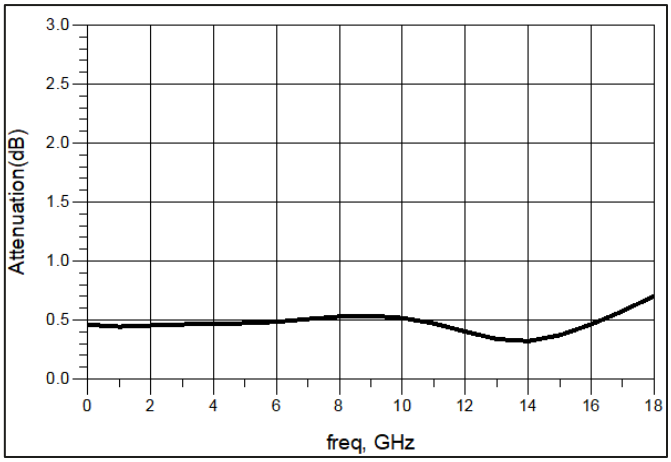


Typical Performance (Post-layout Simulations)

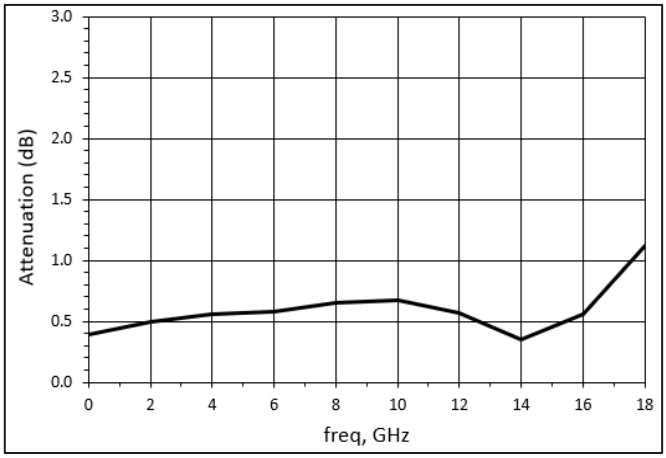
Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

Relative attenuation error –Major state(RMS)

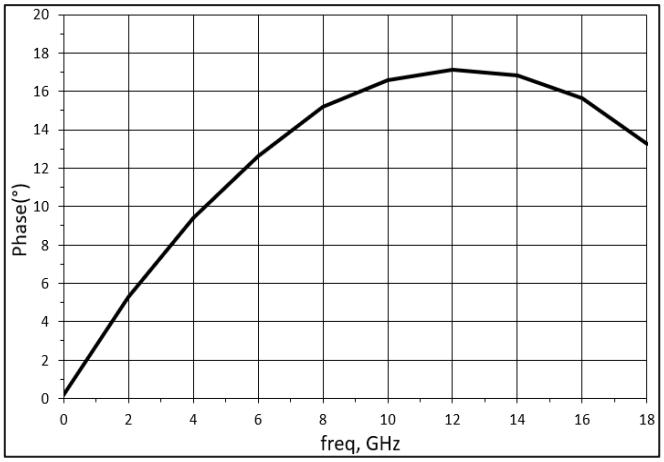


Relative attenuation error –Major state(MAX)



Relative Phase error –Major state(RMS)

Relative Phase error –Major state(MAX)

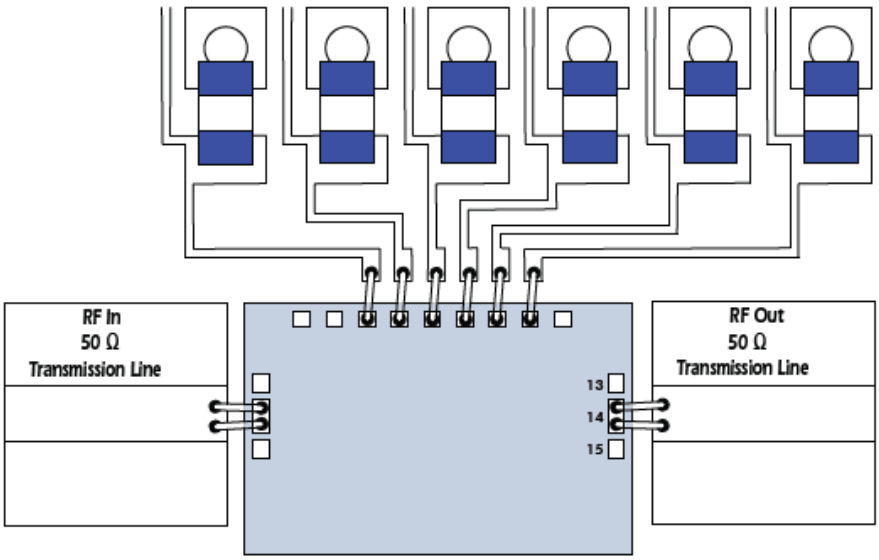


Typical Performance (Post-layout Simulations)

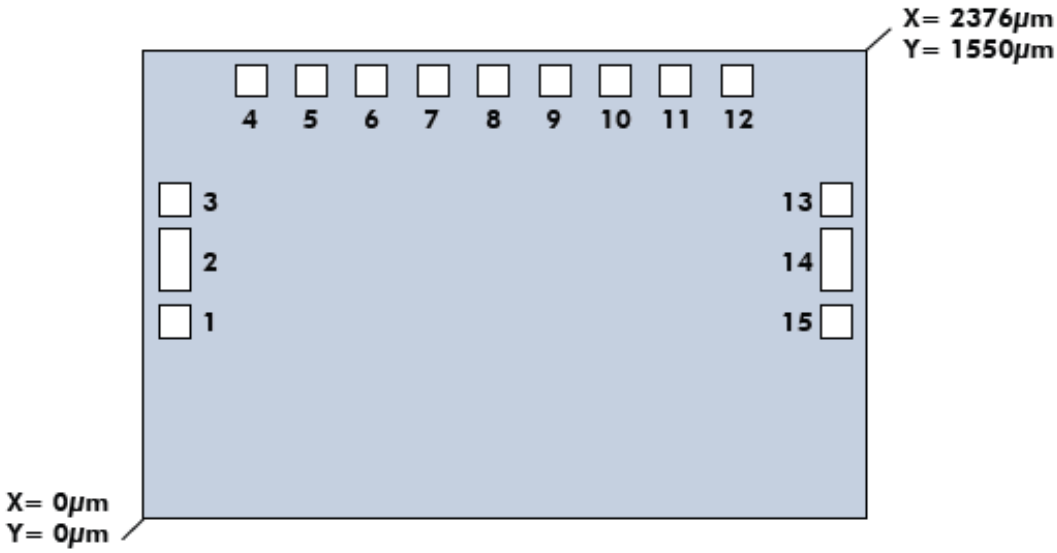
Attenuation Level(dB)	Vc1	Vc2	Vc3	Vc4	Vc5
0 (Reference state)	0	0	0	0	0
0.9	1	0	0	0	0
1.8	0	1	0	0	0
3.6	0	0	1	0	0
7.2	0	0	0	1	0
14.4	0	0	0	0	1
27.9	1	1	1	1	1

Biasing:

On each control PAD (Vc1 to Vc5), a decoupling capacitor and a source resistance can be used. Choose adequate component not to deteriorate dynamic switching performances. For example, each DC/Control pad (Vss and Vc1 to Vc5) can have DC bypass capacitance (about 100pF) as close to the device as possible. Alternatively, place 100pF multi-layer ceramic capacitors close to the die as shown hereafter.



Die layout



Pinout and Bonding Pad Co-ordinates

Die Pin Out						
Pad	X (µm)	Y (µm)	Size (µm x µm)	Name	Value	Function
1	100	658	100x100	GND		
2	100	858	100x200	RF In		
3	100	1058	100x100	GND		
4	347	1450	100x100	GND		
5	547	1450	100x100	Ref_A		
6	747	1450	100x100	Vc1	0/3V	0.9dB Attenuation Bit
7	947	1450	100x100	Vc2	0/3V	1.8dB Attenuation Bit
8	1147	1450	100x100	Vc3	0/3V	3.6dB Attenuation Bit
9	1347	1450	100x100	V_{SS}	-7.5V	Bias Voltage
10	1547	1450	100x100	Vc4	0/3V	7.2dB Attenuation Bit
11	1747	1450	100x100	Vc5	0/3V	14.4dB Attenuation Bit
12	1947	1450	100x100	Ref_B		
13	2276	858	100x100	GND		
14	2276	858	100x200	RF Out		
15	2276	858	100x100	GND		

Die Thickness= 100µm
Die bottom must be connected to the ground (RF and DC)

Ordering Information

Product code	Definition
VM103D	DC to 18 GHz/ 5-Bit Digital Attenuator in Die form

Associated Material

Product Code	Definition
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit expo-sure to temperature above 300° C during 3-4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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