7 to 13 GHz 6 Bit Phase Shifter

DATA SHEET PRELIMINARY VM104D

General Description

The **VM104D**, is a wide band GaAs MMIC
- 6-bit phase shifter
- Digital control logic

The digital control logic allows for parallel data input, so phase shifter may be changed instantaneously.

This Digital Phase Shifter has an LSB of 5.6 Degree and controlled by 6 digital binary inputs, compatible with LVCMOS levels. This device uses a single -7.5 V Bias supply voltage.

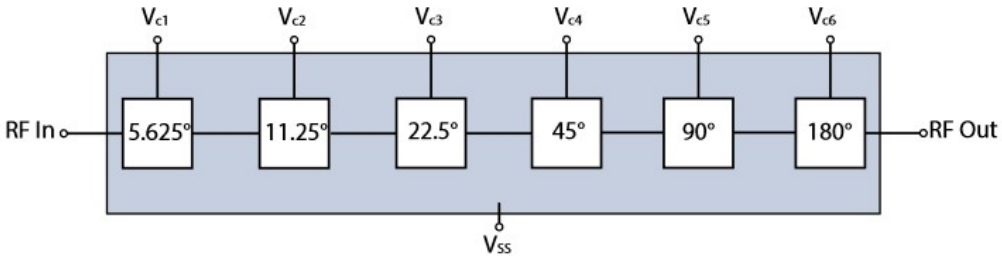
Typical Features

- Operating frequency range: 7 to 13GHz
- 6-bit Phase shifter
- LSB 5.625 Degree
- 26 dBm P1dB input compression
- Digital control (0 / + 3 V)
- Parallel data input
- Chip size: 3.0 x 2.1 x 0.1 (mm)

Applications

- Active Antenna
- RF Communication
- RF Front end
- Test and Measurement

Pin Assignment & Functional Block Diagram



Symbol	Pad N°
RF In	2
V_{C1}	6
V_{C2}	7
V_{C3}	8
V_{SS}	9
V_{C4}	10
V_{C5}	11
V_{C6}	12
RF Out	15

Electrical Specifications

Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	7		13	GHz
LSB	6 Bit Phase Shifter - Resolution		5.625		Deg
IL	Insertion Loss @ 10 GHz (Reference state)		6.6		dB
S11	Input Return loss (All states)		-12		dB
S22	Output Return loss (All states)		-14		dB
Input P_{1dB}	Input Power @ 1 dB		26		dBm
RMS A	RMS Attenuation Error		0.5		dB
RMS P	RMS Phase Error		3		Deg
P Error	Max Phase Error		10		Deg
ST/SF	Switching speed		TBD		ns
V_{SS}	Supply Voltage		-7.5		VDC
I_{SS}	Supply Current		12		mA
Vci_H	Bit control voltage High	2.5	3	5	V
Vci_L	Bit control voltage Low	0		0.8	V

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{SS}	Supply Voltage	-15		V
Pin	CW RF input power		30	dBm
T process	Soldering temperature		300	°C
Tch	Channel temperature(*)		150	°C
Ta	Operating temperature range	-40	+85	°C
Tstg	Storage temperature range	-55	+150	°C

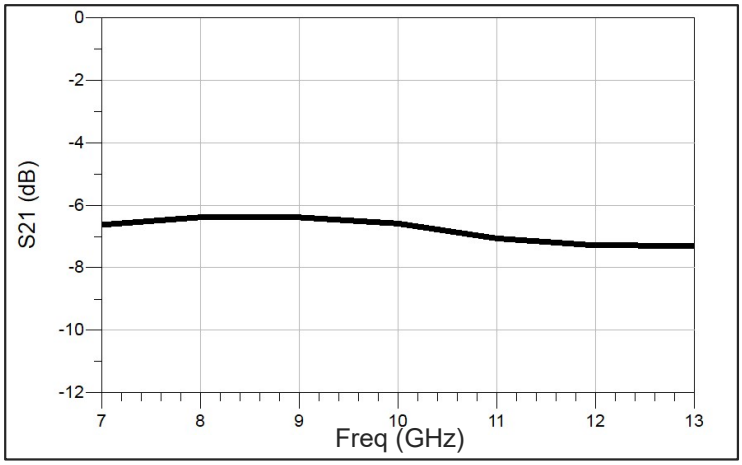
(*)Rth, thermal resistance from junction to backside: TBD
Operation of this device above any of these parameters may cause permanent damage.

Typical Performance (Post-layout Simulations)

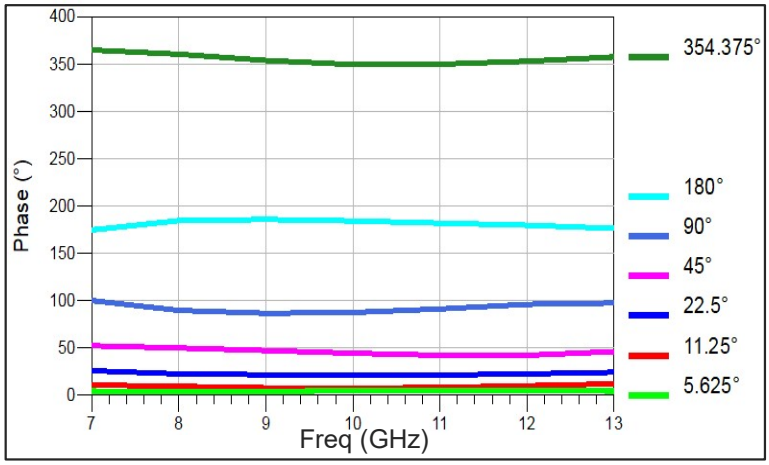
Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

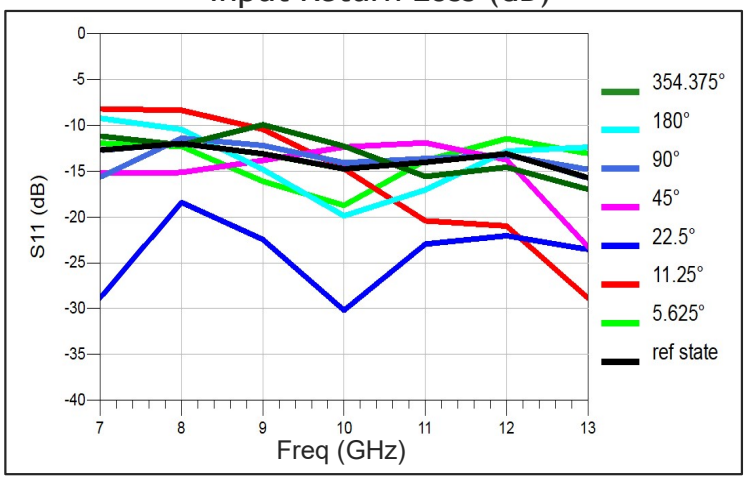
Reference State-insertion loss(dB)



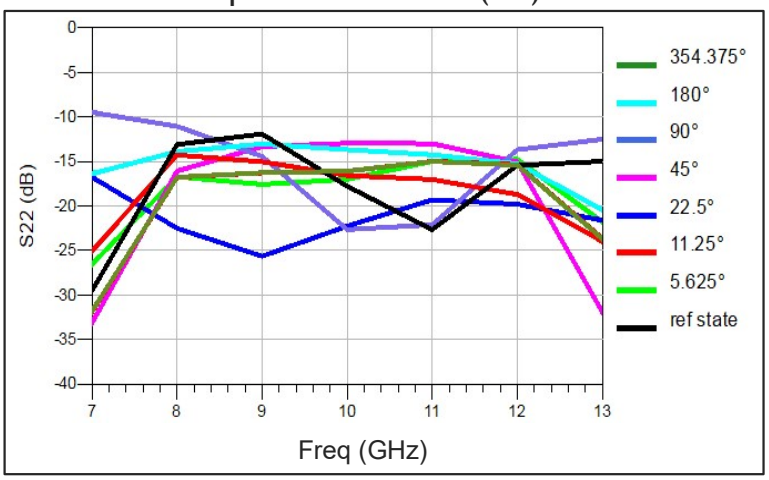
Absolute Relative phase- Major state(deg)



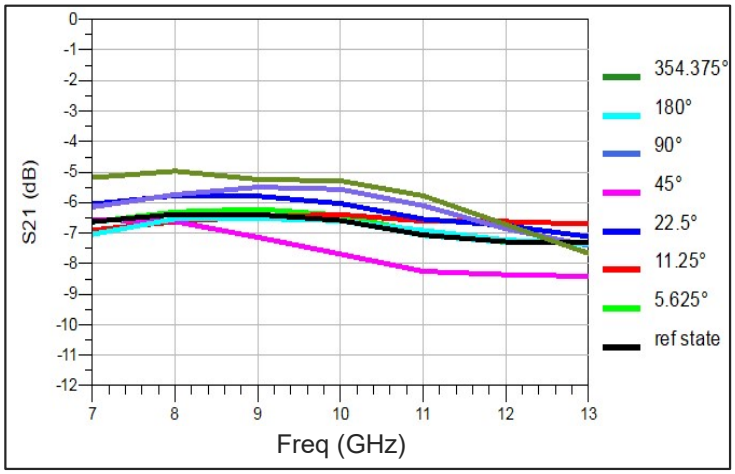
Input Return Loss (dB)



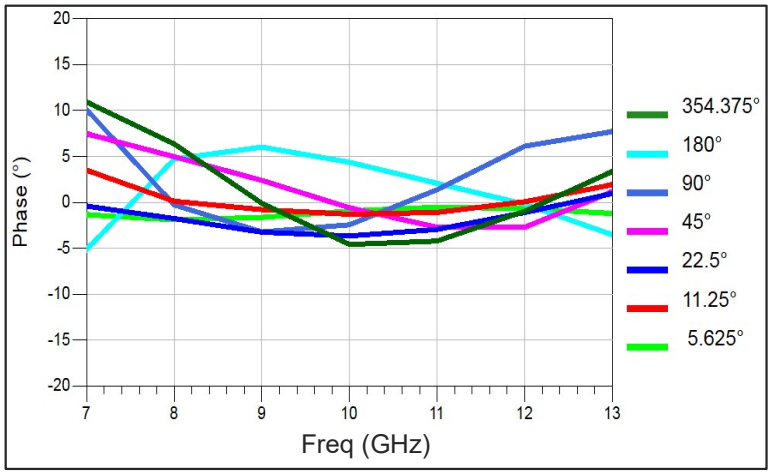
Output Return Loss (dB)



Attenuation level - Major state(dB)



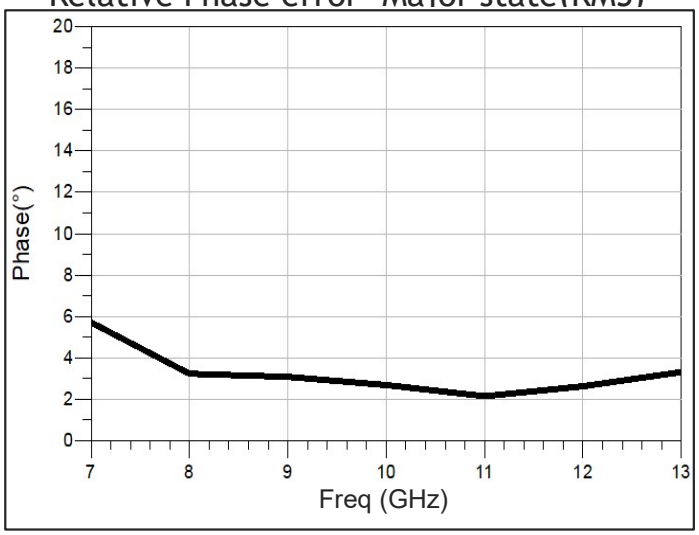
Bit error- Major state(deg)



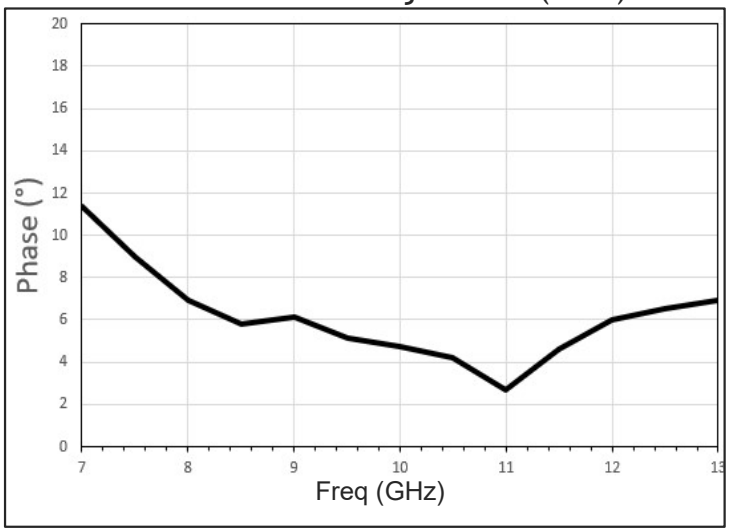
Simulation conditions unless otherwise noted:

- Tamb. = +25° C
- Vss = -7.5V

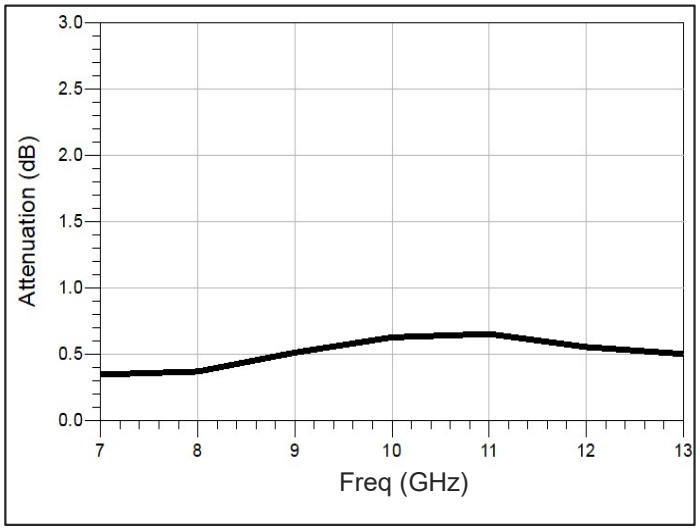
Relative Phase error -Maior state(RMS)



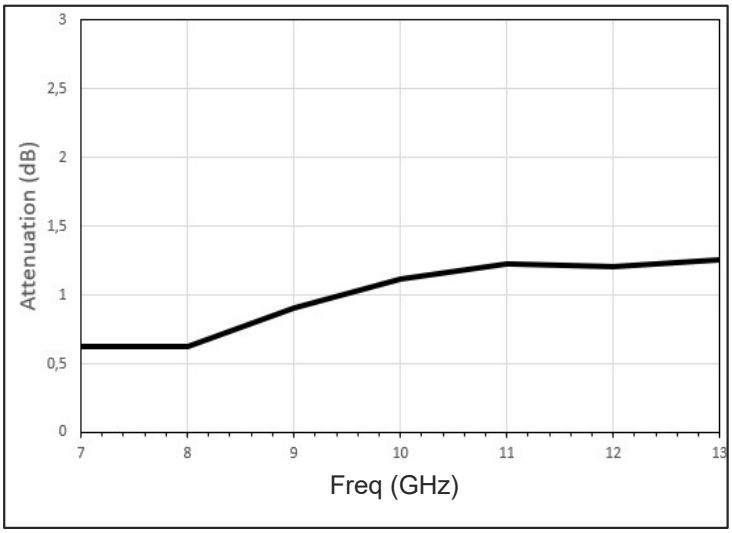
Relative Phase error -Major state(MAX)



Relative attenuation error -Major state(RMS)



Relative attenuation error -Major state(MAX)

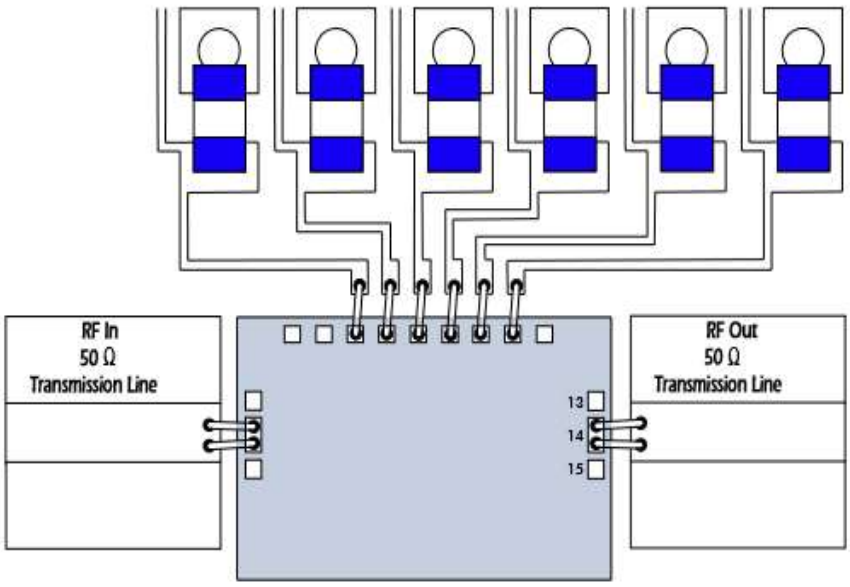


Logic truth table (Major State)

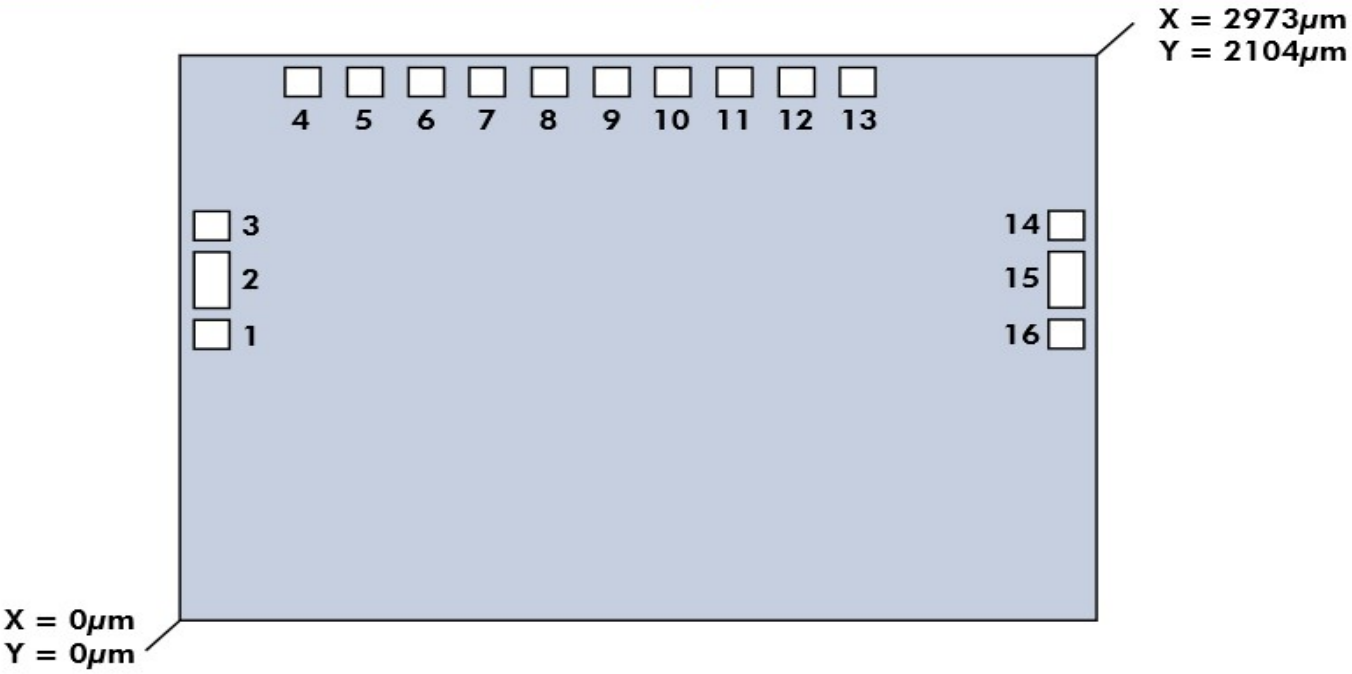
Phase Shift (Degrees)	Vc1	Vc2	Vc3	Vc4	Vc5	Vc6
0 (reference state)	0	0	0	0	0	0
5.625	1	0	0	0	0	0
11.25	0	1	0	0	0	0
22.5	0	0	1	0	0	0
45	0	0	0	1	0	0
90	0	0	0	0	1	0
180	0	0	0	0	0	1
354.375	1	1	1	1	1	1

Typical Assembly Diagram

On each control PAD (Vc1 to Vc6), a decoupling capacitor and a source resistance can be used. Choose adequate component not to deteriorate dynamic switching performances.
For example, each DC/Control pad (Vss and Vc1 to Vc6) can have DC bypass capacitance (about 100pF) as close to the device as possible. Alternatively, place 100pF multi-layer ceramic capacitors close to the die as shown hereafter.



Die Layout



Pinout and Bonding Pad Coordinates

Die Pin Out						
Pad	X (µm)	Y (µm)	Size (µm x µm)	Name	Value	Function
1	100	1067	100x100	GND		
2	100	1267	100x100	RF In		
3	100	1467	100x100	GND		
4	398	2000	100x100	GND		
5	598	2000	100x100	Ref_A		
6	798	2000	100x100	V_C1	0/+3V	5.625° Phase Bit
7	998	2000	100x100	V_C2	0/+3V	11.25° Phase Bit
8	1198	2000	100x100	V_C3	0/+3V	22.5° Phase Bit
9	1398	2000	100x100	V_{SS}	-7.5V	Supply Voltage
10	1598	2000	100x100	V_C4	0/+3V	45° Phase Bit
11	1798	2000	100x100	V_C5	0/+3V	90° Phase Bit
12	1998	2000	100x100	V_C6	0/+3V	180° Phase Bit
13	2198	2000	100x100	Ref_B		
14	2873	1467	100x100	GND		
15	2873	1267	100x100	RF Out		
16	2873	1067	100x100	GND		

Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

Product code	Definition
VM104D	PSH/GaAs 7-13GHz 6bits PhSh LPS 5.625° MPS 354.375° Die

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
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Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 ° C during 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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