# 8.5 to 11GHz X-Band Core-Chip

**DATA SHEET** **VWA 5000049 AA**

## General Description

The **VWA5000049AA** integrates:
- Transmit and receive switches
- LNA, MPA, inter-stage amplifiers
- 6-bit phase shifter
- 5-bit attenuator
- Digital control logic

The digital control logic allows for parallel data input, so phase shifter and attenuator may be changed instantaneously.

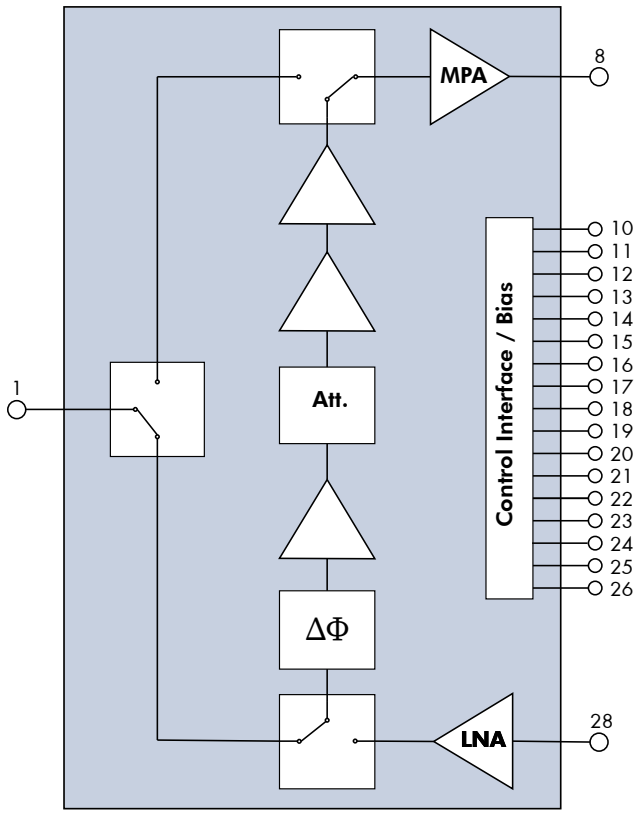
## Features

- Operating frequency range: 8.5 to 11GHz
- Receive and Transmit mode operation
- Receive linear typical gain: 20dB
- Transmit linear typical gain: 24dB
- 20dBm Tx P1dBc
- 5.2dB Rx Noise figure
- 6 bits phase shifter: 0-360° (step 5.625°)
- 5 bits attenuator: 0-27.9 dB (step 0.9dB)
- Parallel data input control logic
- Chip size: 5.0 x 4.0 x 0.1 (mm)

## Applications

- RZ Pulsed shape driver
- 10GBps Communication systems.
- Active Antenna.
- Telecom Clock Management

## Pins Assignement & Functional Block Diagram




| Symbol | Pad N° |
|---|---|
| Tx/Rx | 1 |
| Tx Out | 8 |
| Rx Out | 28 |

# Electrical Specifications

**Test conditions unless otherwise noted:**

- Tamb.= +25°C

| Symbol | DC Features | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$ | Drain bias voltage | | 4.0 | 4.5 | V | |
| $I_D$ | Drain current : Tx mode | | 280 | | mA | 1 |
| $V_{S1}$, $V_{S2}$, $V_{S3}$, | Gate bias voltage | | -5.0 | | V | 1 |
| $I_G$ | Gate current | | 35 | | mA | |
| Hight level | Control voltage : Va & Vp | 2.0 | 3.3 | 5.0 | V | |
| Low level | | 0 | | 0.8 | V | |
| $V_I$ | Load pull | 2.0 | 3.3 | 5.0 | V | |
| $I_I$ | Load pull current | | 9.5 | | mA | |

| RF Spécifications | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency range | | 8.5 | | 11 | GHz |
| Input return loss | Rx/Tx mode | -9.5 | | | dB |
| Output return loss | Rx/Tx mode | -12 | | | dB |
| Phase shifter range : 6 bits | | 0 | | 360 | ° |
| RMS phase error | | | 1.5 | 3.5 | ° |
| Attenuator range | | 0 | | 27.9 | dB |
| RMS amplitude error | | | 0.3 | 0.6 | dB |
| Receive mode (reference state, all phase & attenuation bits at 0) | | | | | |
| Small signal gain | | 18 | 20 | | dB |
| Output power (1dB compression point) | | 17 | 18 | | dBm |
| Noise figure | | | 5.2 | | dB |
| Transmit mode (reference state, all phase & attenuation bits at 0) | | | | | |
| Small signal gain | | 21 | 24 | | dB |
| Output power (1dB compression point) | | 20 | 22 | | dBm |

Note 1: The parameters value are controlled on standard production wafer measurement for four frequencies 9GHz, 9.5GHz, 10GHz, 10.5GHz.

| RF Spécifications | Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Frequency range | | 9 | | 10.5 | GHz | |
| Input return loss | Rx/Tx mode | -11 | | | dB | |
| Output return loss | Rx/Tx mode | -14 | | | dB | |
| Phase shifter range : 6 bits | | 0 | | 360 | ° | |
| RMS phase error | | | 1.5 | 2.5 | ° | |
| Attenuator range | | 0 | | 27.9 | dB | |
| RMS amplitude error | | | 0.3 | 0.6 | dB | |
| Receive mode (reference state, all phase & attenuation bits at 0) | | | | | | |
| Small signal gain | | 19 | 20 | | dB | 1 |
| Output power (1dB compression point) | | 17 | 18 | | dBm | |
| Noise figure | | | 5.2 | | dB | |
| Transmit mode (reference state, all phase & attenuation bits at 0) | | | | | | |
| Small signal gain | | 23 | 24 | | dB | 1 |
| Output power (1dB compression point) | | 21 | 22 | | dBm | |

## Absolute Maximum Ratings

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$ | Drain bias voltage | | | +6.0 | V |
| $V_{S1}$, $V_{S2}$, $V_{S3}$ | Gate bias voltage | | | -4.0 | V |
| VI | Logic voltage | -6.0 | | +5.5 | V |
| $I_D$ | Drain current | | | 350 | mA |
| | Input power : Rx mode | | | +15 | dBm |
| | Input power : Tx mode | | | +15 | dBm |
| Tst | Storage temperature | -65 | | +165 | °C |
| Top | Operating temperature (back of the die) | -55 | | MTTF(*) | °C |

*(*) : Channel temperature affects the device's MTTF. see MTTF graphs*

Note 1: The parameters value are controlled on standard production wafer measurement for four frequencies 9GHz, 9.5GHz, 10GHz, 10.5GHz.

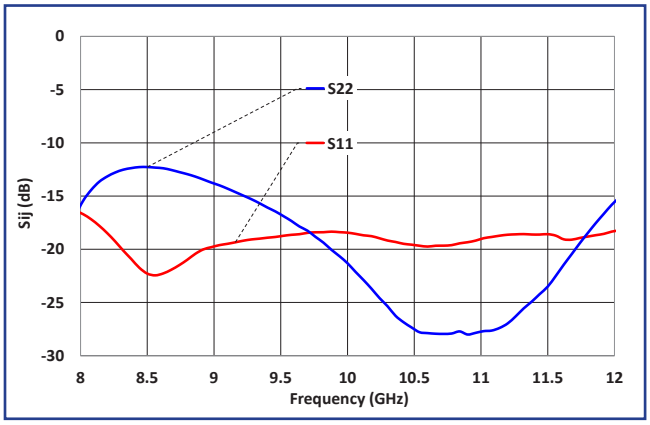
# Typical Performance (Test Under Probes)

**Test conditions unless otherwise noted:**

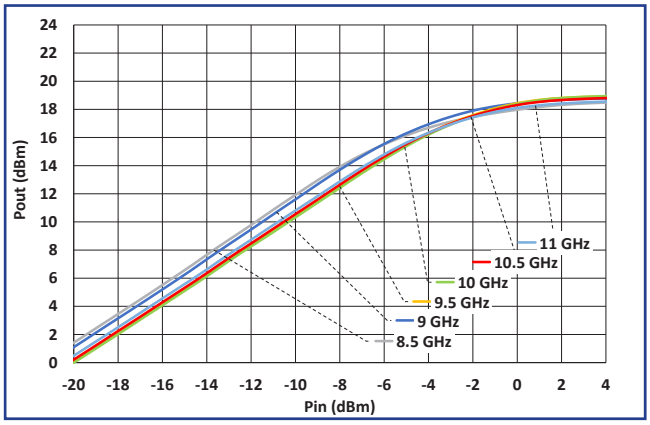
- Tamb.= +25°C

## Rx Mode

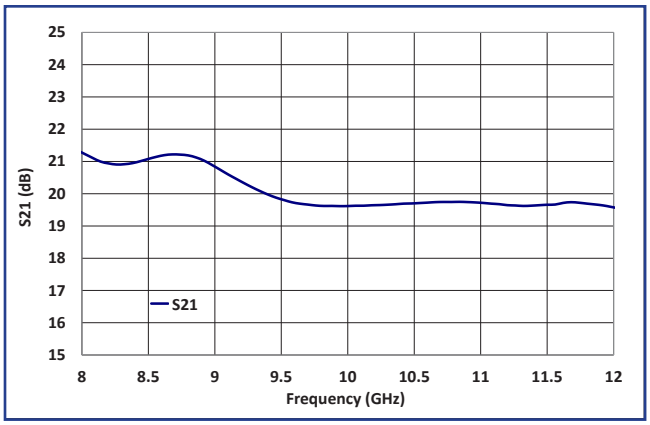
### Input & Output Return Losses



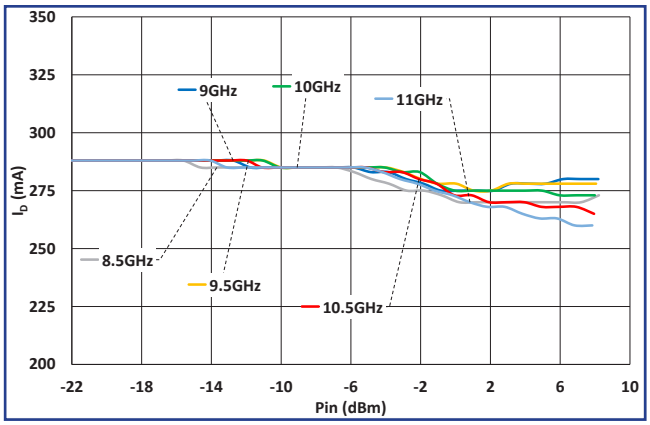

### Output Power vs Input Power for various Frequency



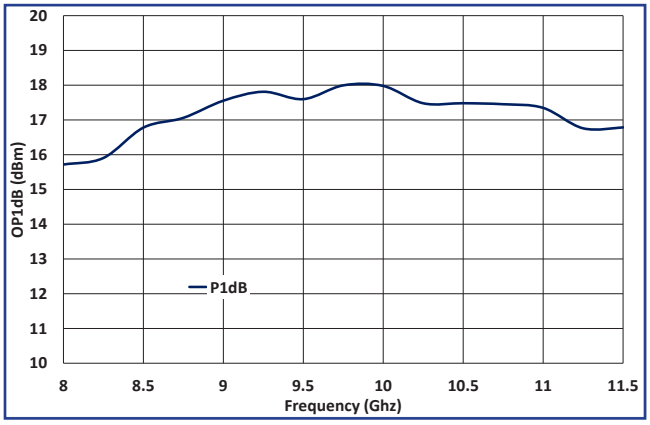

### Small Signal Gain



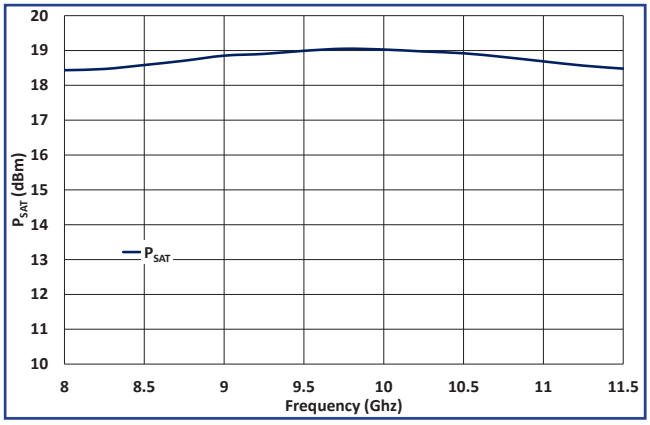

### Drain Current vs Input Power vs for various Frequency




### Output P1dB




### Saturated Output Power



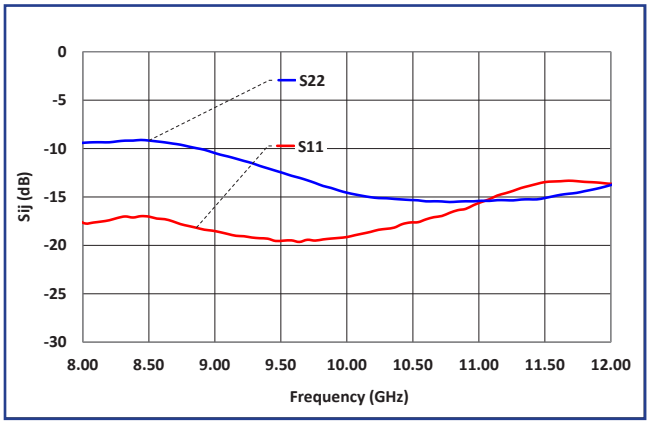
# Typical Performance (Test Under Probes)

**Test conditions unless otherwise noted:**

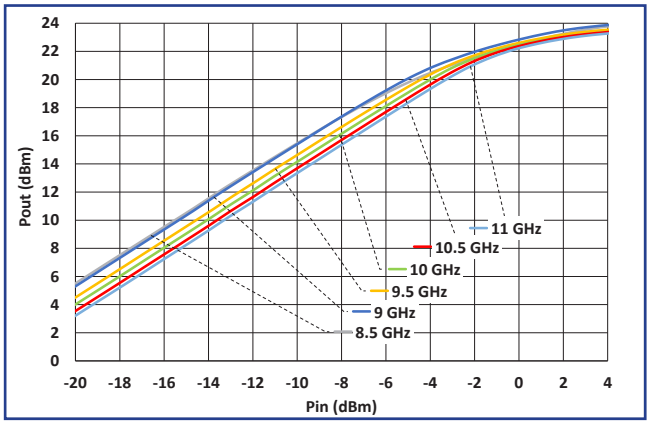
- Tamb.= +25°C

## Tx Mode

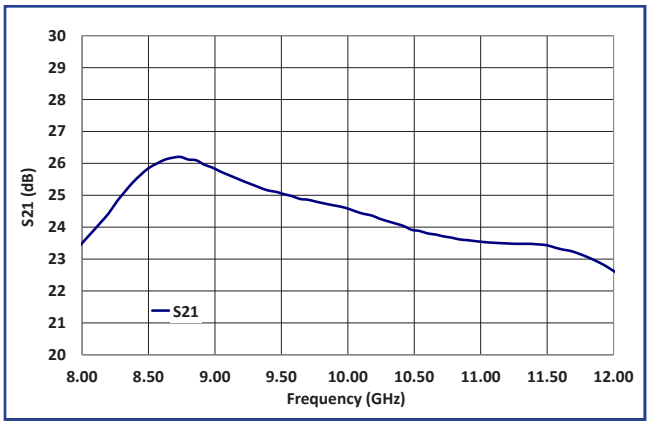
### Input & Output Return Losses



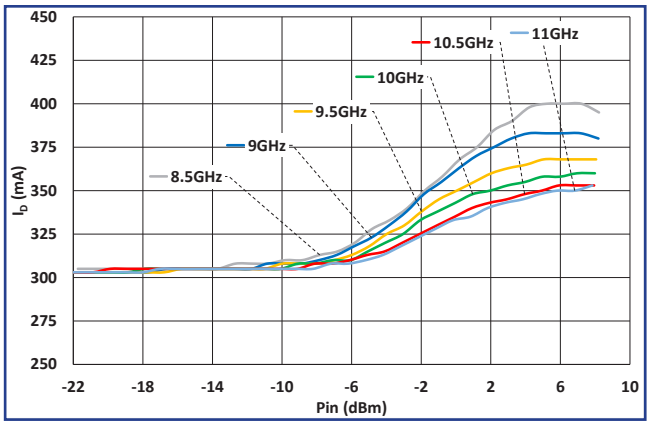

### Output Power vs Input Power for various Frequency



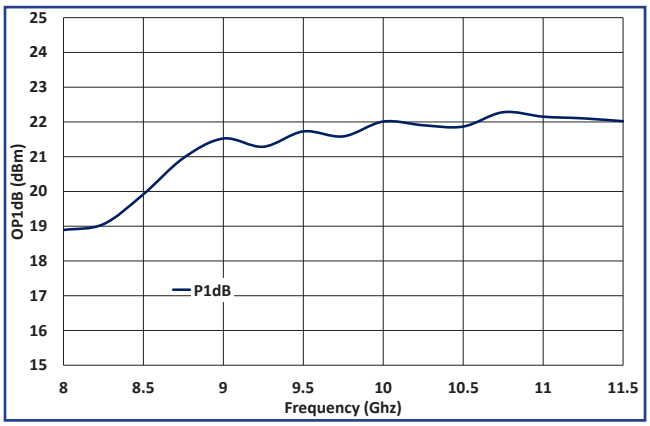

### Small Signal Gain



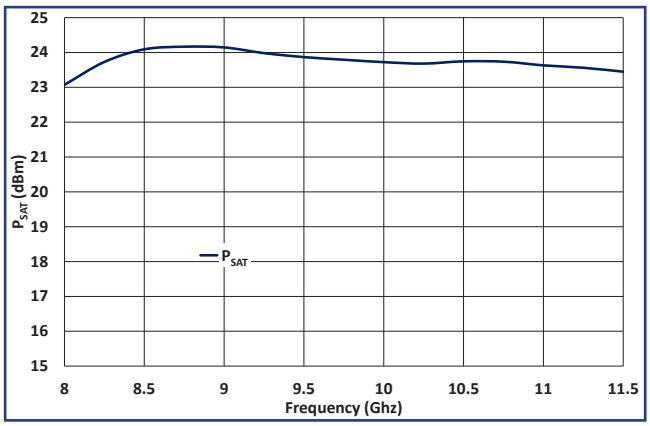

### Drain Current vs Input Power vs for various Frequency




### Output P1dB

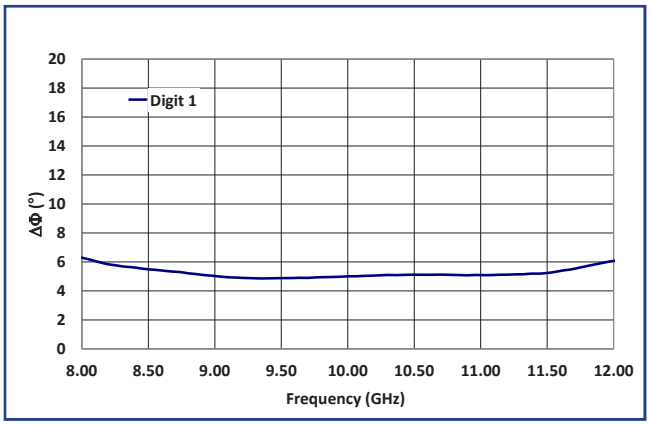



### Saturated Output Power

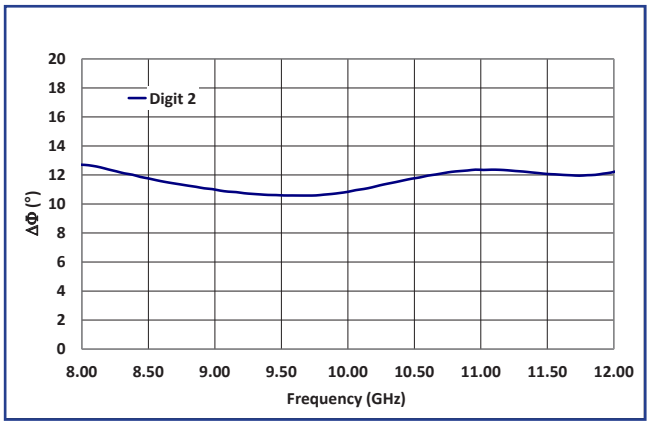


# Phase Shifter Accuracy

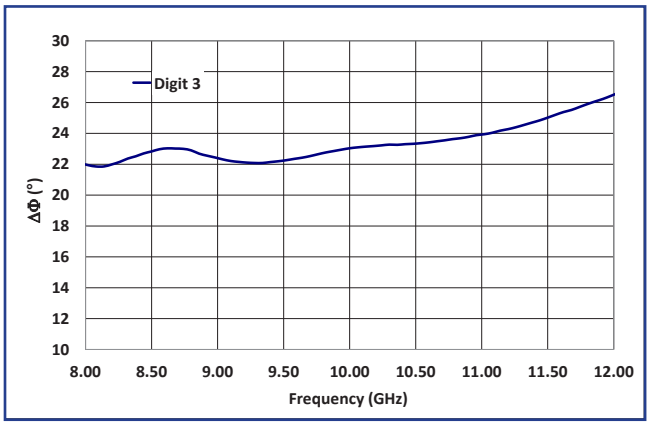
### Phase Shift (°) : Digit 1



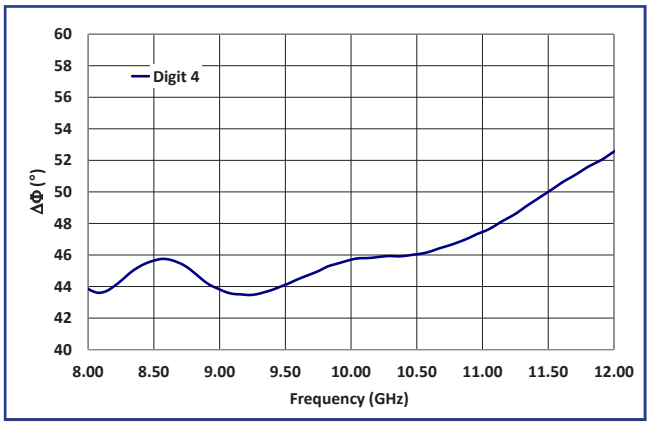

### Phase Shift (°) : Digit 2



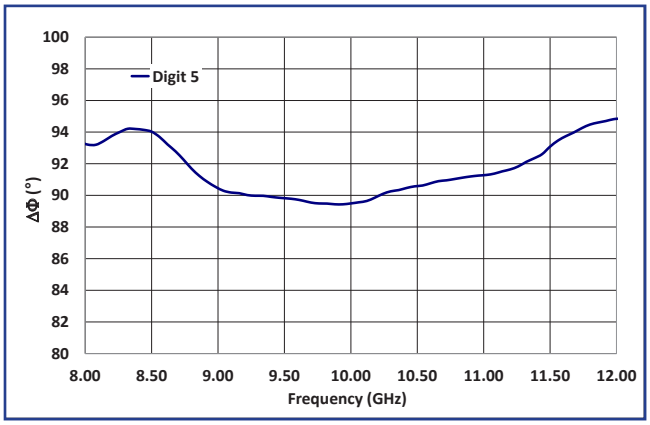

### Phase Shift (°) : Digit 3



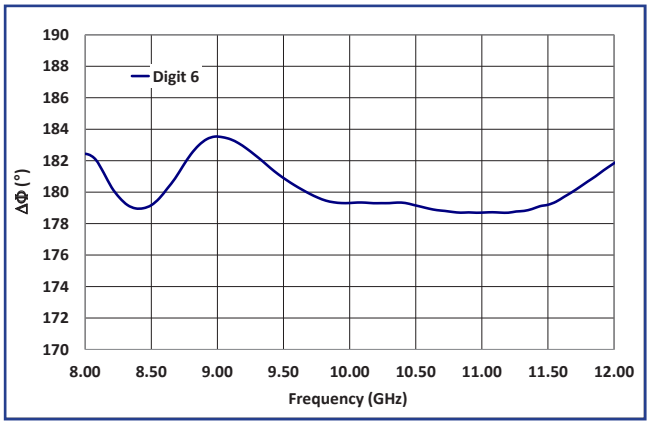

### Phase Shift (°) : Digit 4




### Phase Shift (°) : Digit 5

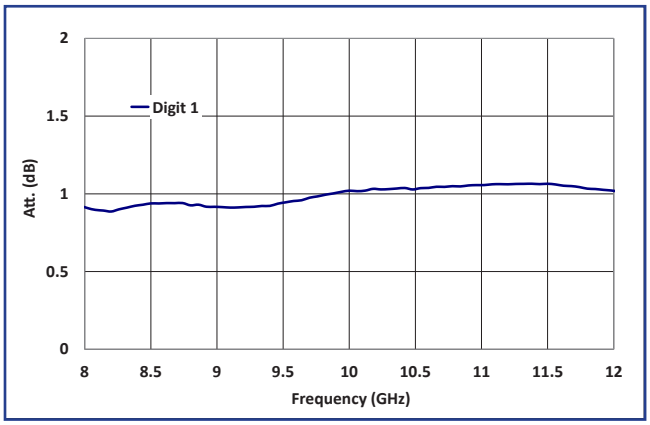



### Phase Shift (°) : Digit 6

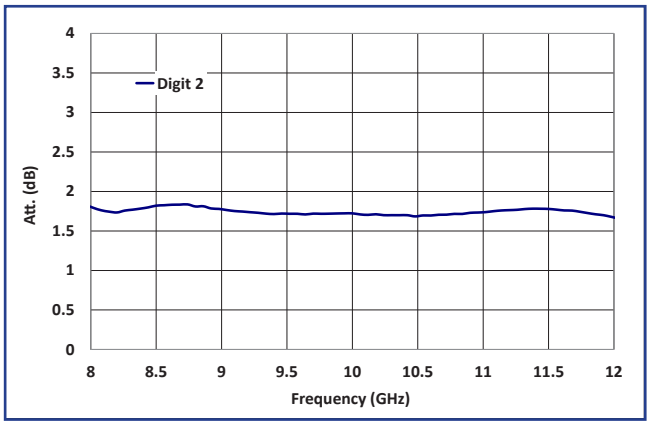


# Attenuator Accuracy

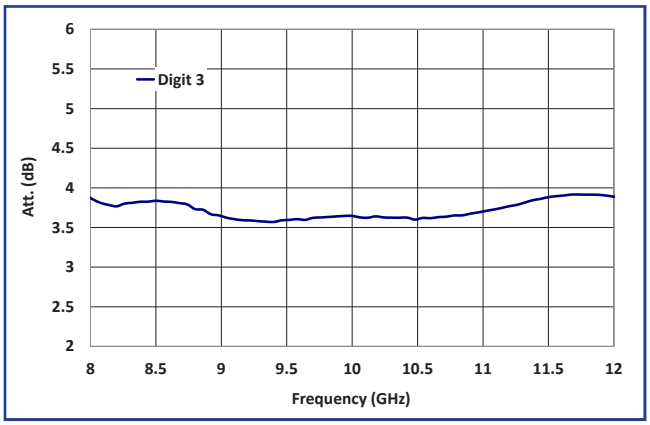
### Attenuation (°) : Digit 1



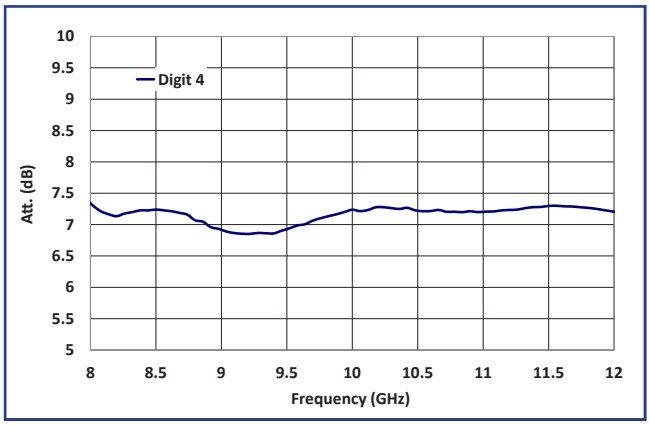

### Attenuation (°) : Digit 2



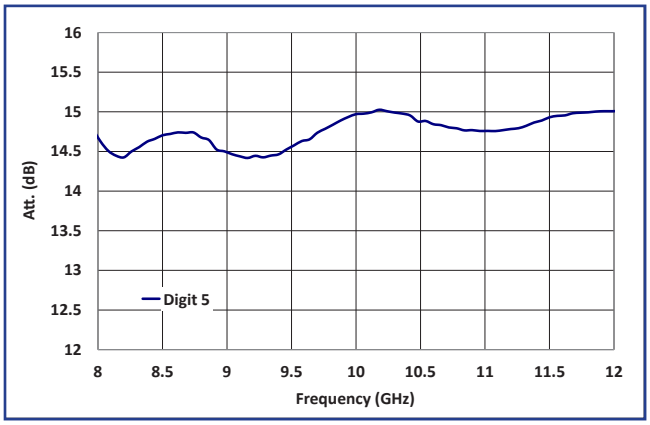

### Attenuation (°) : Digit 3




### Attenuation (°) : Digit 4




### Attenuation (°) : Digit 5



# Using Informations

- ***Decoupling and Assembly recommendations***

Bond wires need to be as short as possible : inductance < 0.13nH for RF accesses.
$V_{D1}$, $V_{D2}$ & $V_{D3}$ : on each, a 100pF single layer capacitor as close as possible to the die.

- ***Biasing***

Negative gate -5V bias ($V_{S1}$, $V_{S2}$ & $V_{S3}$) must be applied before positive voltages ($V_{D1}$, $V_{D2}$, $V_{D3}$ & $V_{D4}$).

In Rx mode :
- Rx_S (pad 14) to logic low :0V: command of the Tx/Rx switch.
- $V_{D2}$ &$V_{D4}$ to +4V: common amplifiers.
- $V_{D1}$ to +4V: LNA
- $V_{D3}$ to 0V: switch off of the MPA.

In Tx mode :
- Rx_S (pad 14) to logic high: +3.3V: command of the Tx/Rx switch.
- $V_{D2}$ &$V_{D4}$ to +4V: common amplifiers.
- $V_{D3}$ to +4V: MPA
- $V_{D1}$ to 0V: switch off of the LNA.

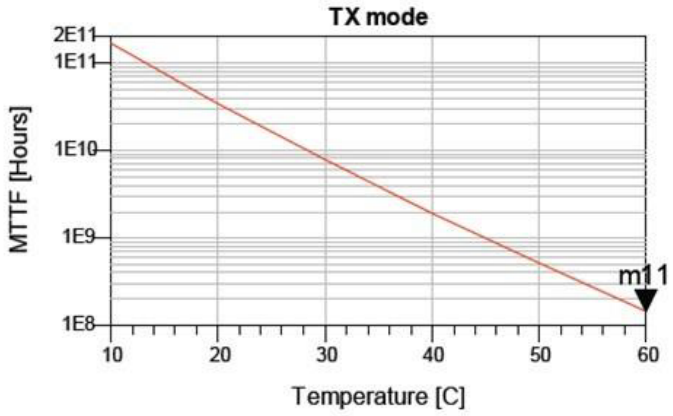
- ***Logic truth table***

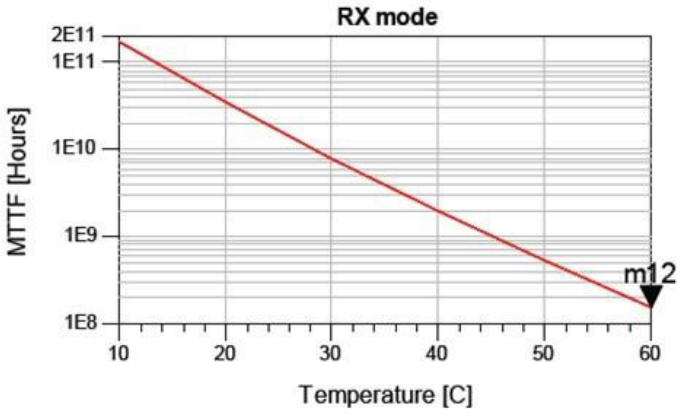
| Attenuator | | | | | |
|---|---|---|---|---|---|
| **Level** | **A1** | **A2** | **A3** | **A4** | **A5** |
| 0 dB | 0 | 0 | 0 | 0 | 0 |
| 0.9 dB | 1 | 0 | 0 | 0 | 0 |
| 1.8 dB | 0 | 1 | 0 | 0 | 0 |
| 3.6 dB | 0 | 0 | 1 | 0 | 0 |
| 7.2 dB | 0 | 0 | 0 | 1 | 0 |
| 14.4 dB | 0 | 0 | 0 | 0 | 1 |
| 27.9 dB | 1 | 1 | 1 | 1 | 1 |

| Phase Shifter | | | | | | |
|---|---|---|---|---|---|---|
| **Phase** | **P1** | **P2** | **P3** | **P4** | **P5** | **P6** |
| 0° | 0 | 0 | 0 | 0 | 0 | 0 |
| 5.625° | 1 | 0 | 0 | 0 | 0 | 0 |
| 11.25° | 0 | 1 | 0 | 0 | 0 | 0 |
| 22.5° | 0 | 0 | 1 | 0 | 0 | 0 |
| 45° | 0 | 0 | 0 | 1 | 0 | 0 |
| 90° | 0 | 0 | 0 | 0 | 1 | 0 |
| 180° | 0 | 0 | 0 | 0 | 0 | 1 |
| 354.375° | 1 | 1 | 1 | 1 | 1 | 1 |

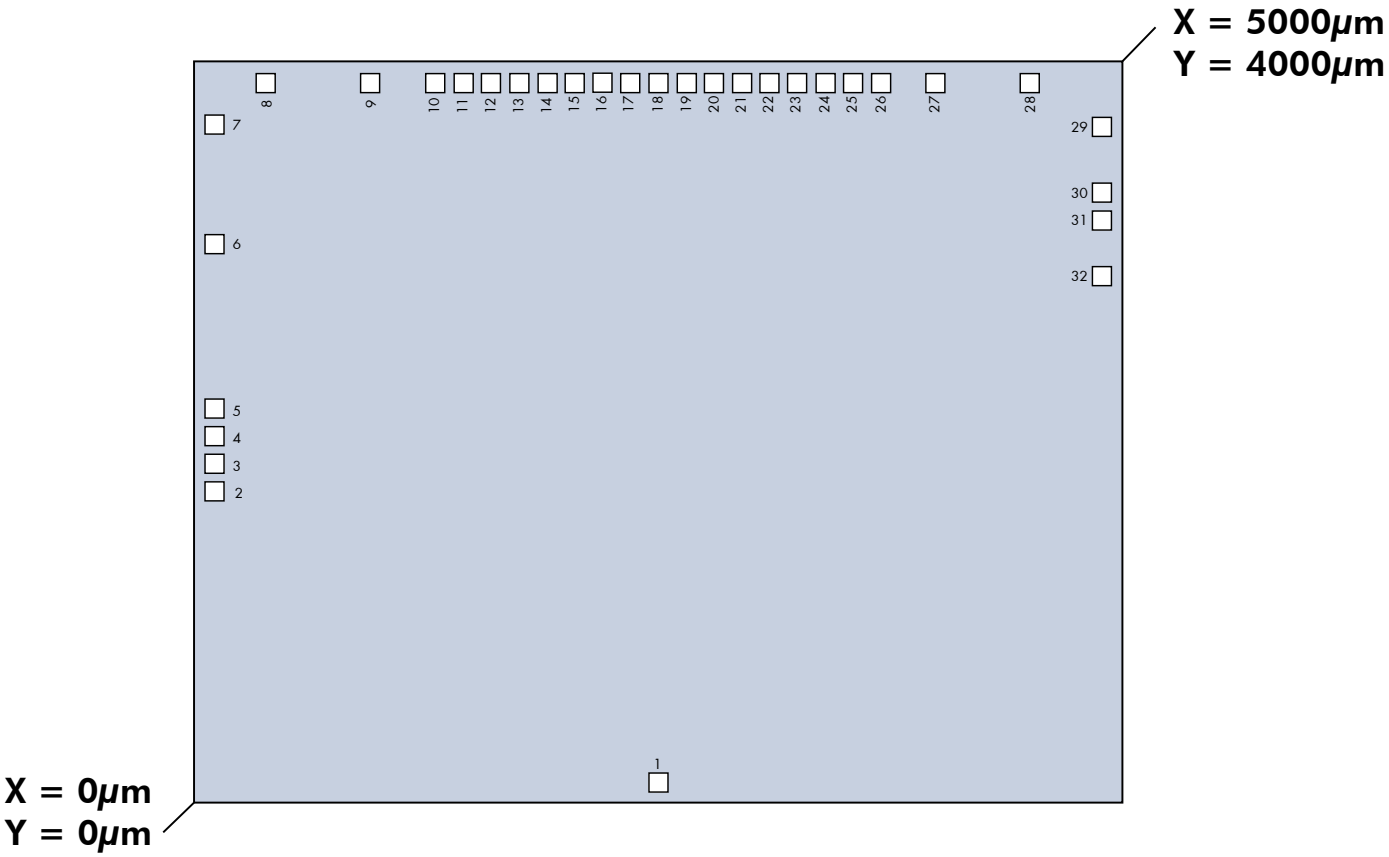
## MTTF graphs

The following graphs give the information based on accelerated life test and thermal model analysis received from the foundry.




## Die Layout




Die thickness = 100µm
Die bottom must be connected to ground (RF and DC)

# Pinout and Bonding Pad Coordinates

| Die Pin Out | | | | | | |
|---|---|---|---|---|---|---|
| **Pad** | **X (µm)** | **Y (µm)** | **Size (µm x µm)** | **Function** | | |
| 1 | 2500 | 110 | 100x100 | Tx/Rx | RF | Tx in & Rx out |
| 2 | 110 | 1680 | 100x100 | $V_{D2}$ | +4V | Common amplifiers bias |
| 3 | 110 | 1830 | 100x100 | $V_{S1}$ | -5V | Gate bias |
| 4 | 110 | 1980 | 100x100 | GND | | |
| 5 | 110 | 2130 | 100x100 | Rx Qnot | 0(Rx) | RF switch monitor |
| 6 | 110 | 3013 | 100x100 | $V_{D3}$ | 0/+4V | RF switch monitor |
| 7 | 110 | 3663 | 100x100 | GND | | |
| 8 | 387 | 3890 | 100x100 | Tx | RF | Tx out |
| 9 | 949 | 3890 | 100x100 | GND | | |
| 10 | 1300 | 3890 | 100x100 | A0 | 0/+3.3V | Atten. Bit 1 : 0.9 dB |
| 11 | 1450 | 3890 | 100x100 | A3 | 0/+3.3V | Atten. Bit 4 : 7.2 dB |
| 12 | 1600 | 3890 | 100x100 | A4 | 0/+3.3V | Atten. Bit 5 : 14.4 dB |
| 13 | 1750 | 3890 | 100x100 | A2 | 0/+3.3V | Atten. Bit 3 : 3.6 dB |
| 14 | 1900 | 3890 | 100x100 | A1 | 0/+3.3V | Atten. Bit 2 : 1.8 dB |
| 15 | 2050 | 3890 | 100x100 | Rx S | 0/+3.3V | Rx/Tx switch |
| 16 | 2200 | 3890 | 100x100 | GND | | Digital ground |
| 17 | 2350 | 3890 | 100x100 | P5 | 0/+3.3V | Phase shift Bit 6 : 180 |
| 18 | 2500 | 3890 | 100x100 | P2 | 0/+3.3V | Phase shift Bit 3 : 22.5 |
| 19 | 2650 | 3890 | 100x100 | P4 | 0/+3.3V | Phase shift Bit 5 : 90 |
| 20 | 2800 | 3890 | 100x100 | P3 | 0/+3.3V | Phase shift Bit 4 : 45 |
| 21 | 2950 | 3890 | 100x100 | P1 | 0/+3.3V | Phase shift Bit 2 : 11.25 |
| 22 | 3100 | 3890 | 100x100 | P0 | 0/+3.3V | Phase shift Bit 1 : 5.625 |
| 23 | 3250 | 3890 | 100x100 | Qnot P0 | 0V | Ref state. Voltage monitor |
| 24 | 3400 | 3890 | 100x100 | Q P0 | -3.4V | Ref state. Voltage monitor |
| 25 | 3550 | 3890 | 100x100 | $V_{S2}$ | -5V | Gate bias |
| 26 | 3700 | 3890 | 100x100 | $V_3$ | +3.3V | Pull-up [1] |
| 27 | 3994 | 3890 | 100x100 | GND | | Decoupling ground |
| 28 | 4500 | 3890 | 100x100 | Rx | RF | Rx in |
| 29 | 4890 | 3654 | 100x100 | $V_{S3}$ | -5V | Gate bias |
| 30 | 4890 | 3296 | 100x100 | $V_{D4}$ | +4V | Gate bias (>0) |
| 31 | 4890 | 3146 | 100x100 | GND | | Decoupling ground |
| 32 | 4890 | 2846 | 100x100 | $V_{D1}$ | 0/+4V | LNA Bias |

*[1] : V3= 3,3V => Attenuation Maximum & Phase shift Maximum.*
*V3= 0V => Attenuation= 0dB & Phase shift= 0 .*
*V3 not connected Ports Ai & Pi operating.*

## Ordering Information

| Product Code | Definition |
|---|---|
| VWA 5000049 AA | 8.5 to 11GHz / X-band Core Chip |

## Associated Material

| Material | Status |
|---|---|
| Packaged die | Contact factory |
| Die Evaluation Board (die EVB) | Contact factory |
| Packaged die Evaluation Board (packaged die EVB) | Contact factory |
| Mechanical files (DXF) | Contact factory |
| Measurents files (S2P) | Contact factory |

## Product Compliance Information

### Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

### ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

**CAUTION ! ESD-Sensitive device**

### RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

Vectrawave SA
5, rue Louis de Broglie
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France

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Tel sales:+33 (0)2 57 63 00 20

**Represented by**