Power Amplifier

33 to 36GHz - 20W GaN/SiC

DATA SHEET **VWA 5001171 AA**

General Description

The **VWA5001171AA** is a Microwave Monolithic Integrated Circuit (MMIC) designed in HEMT (High Electron Mobility Transistor) structure for operating frequency range from 33 to 36GHz.

The MMIC is developed on a 150nm GaN/SiC process and is internally matched for 50Ω RF accesses. It provides an output power of 20W, and associated Power Added Efficiency of 25% typical in Continuous Wave (CW) or Pulsed mode.

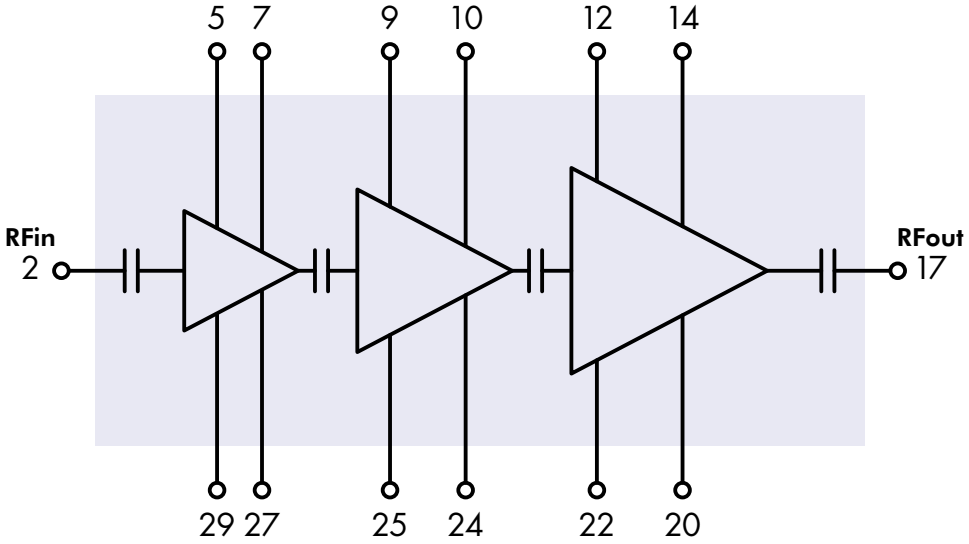
Features

- Operating frequency range: 33 to 36GHz
- Output Power: 43dBm @Pin= 26dBm
- PAE: 22% @Pin= 26dBm
- Linear Gain: 22dB
- DC bias: V_D= +22V, I_{DQ}= 2400mA, V_G= -1.5V (Typical)
- Chip size: 4.86 x 4.44 x 0.1mm

Applications

- **Radar**
- **Military**
- **Telecommunications**

Functional Block Diagram & Pins Assignment



Function	Pin number
RF in	2
RF out	17
VD1A / VD1B	7 / 27
VD2A / VD2B	10 / 24

Function	Pin number
VD3A / VD3B	14 / 20
VG1A / VG1B	5 / 29
VG2A / VG2B	9 / 25
VG3A / VG3B	12 / 22

Electrical Specifications

Test conditions unless otherwise noted:

- ID = 2400mA
- VG = -1.5V Typical
- T_{amb} = +25°C
- Post layout simulation
- VD = 22V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	33		36	GHz
BW	Operating Bandwidth		3		GHz
G	Small signal gain		22		dB
Gp	Power gain		17		dB
S11	Input Return loss		10		dB
S22	Output Return loss		10		dB
P_{OUT}	Output power (Pin=26dBm)		43		dBm
PAE	Power Added Efficiency (Pin=26dBm)		25		%
I_D	Drain current (Pin=26dBm)		4		A
V_D	Drain voltage		22		V
P1dB	P1dB compression		NA		dBm
ΔG	Small signal gain temperature coefficient		NA		dB/°C

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_D	Quiescent drain voltage	22	V
I_{DQ}	Quiescent drain current	2400	mA
V_G	Quiescent gate voltage (Typical)	-1.5	V

Absolute Maximum Ratings

Symbol	Maximum Ratings	Min	Unit
V_D	Drain voltage	28	V
I_D	Maximum saturated drain current	5	A
V_G	Gate voltage	-6 to 0	V
P_{DISS}	Power dissipated (Tcarrier=85°C)	100	W
P_{IN}	Maximum input power	30	dBm
Tj	Junction temperature	225	°C
Ta	Operating temperature	-40/+85	°C
Tstg	Storage temperature	-55/150	°C

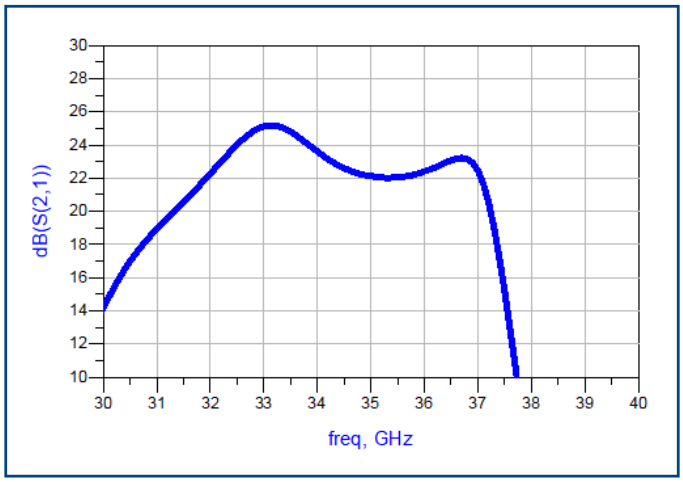
Operation of this device above any of these parameters may cause permanent damage.

Typical performances (Small signal / post-layout simulation)

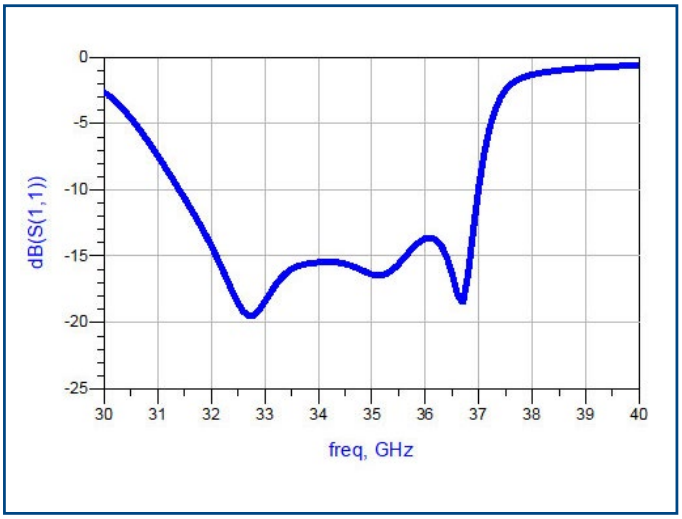
Simulated conditions:

- V_{DD} = +22V
- I_{DQ} = 2.4A
- RF bondings 0.1nH at RFin / RFout
- T_{amb} = +25°C

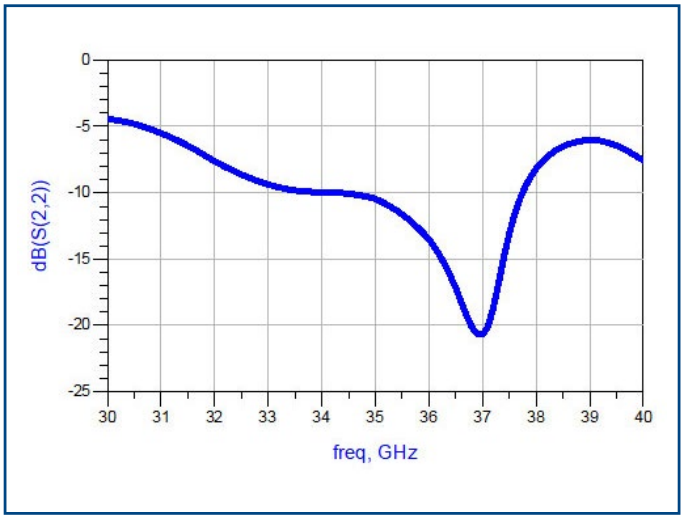
Small Signal Gain (dB)



Input Return Losses (dBm)



Output Return Losses (dBm)

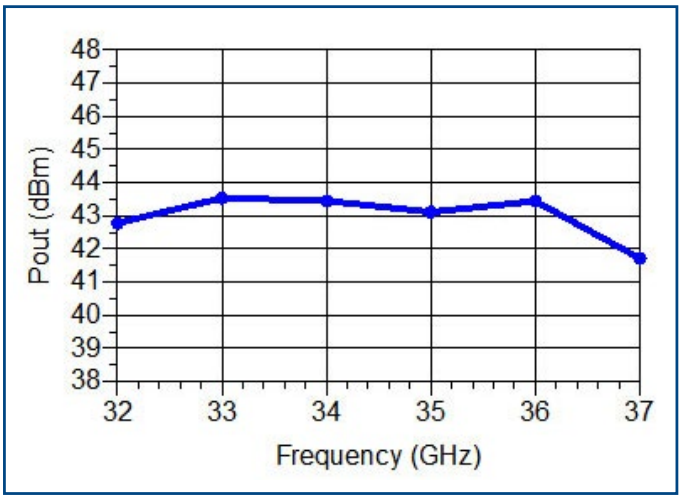


Typical performances (Large signal / post-layout simulation)

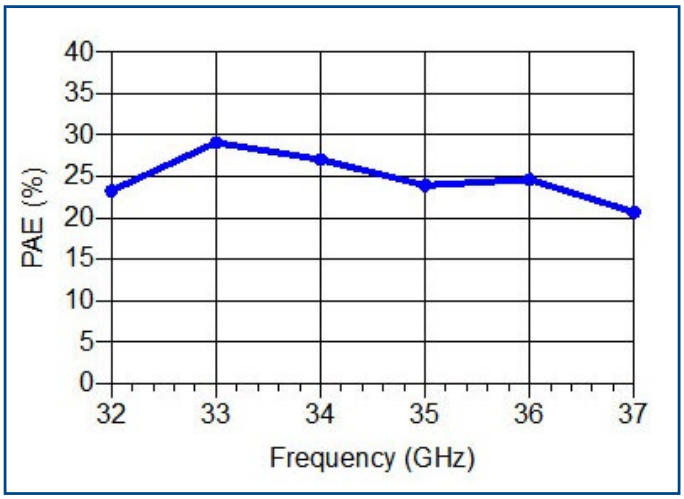
Simulated conditions:

- V_{DD} = +22V
- I_{DQ} = 2.4A
- T_{amb} = +25°C
- RF Pin = +26dBm
- RF bondings 0.1nH at RFin / RFout

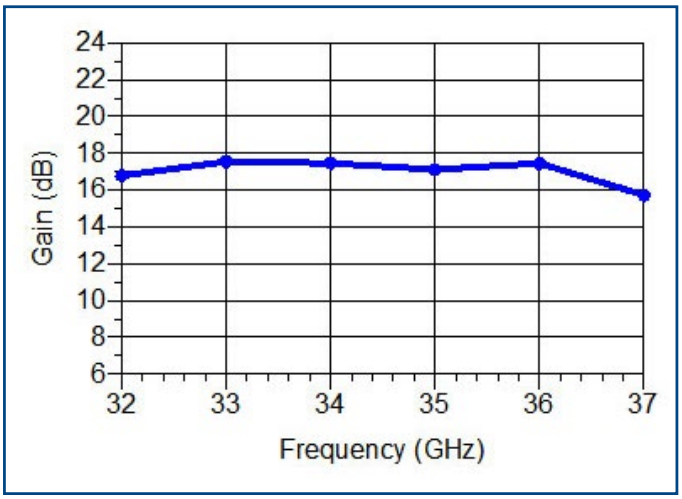
Pout (dBm)



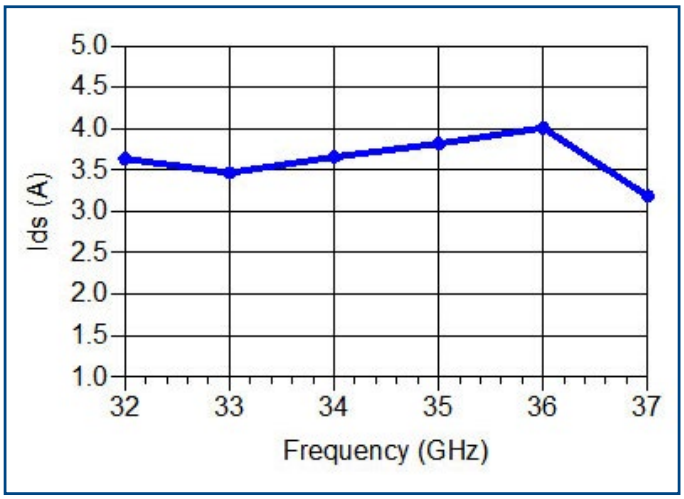
PAE (%)



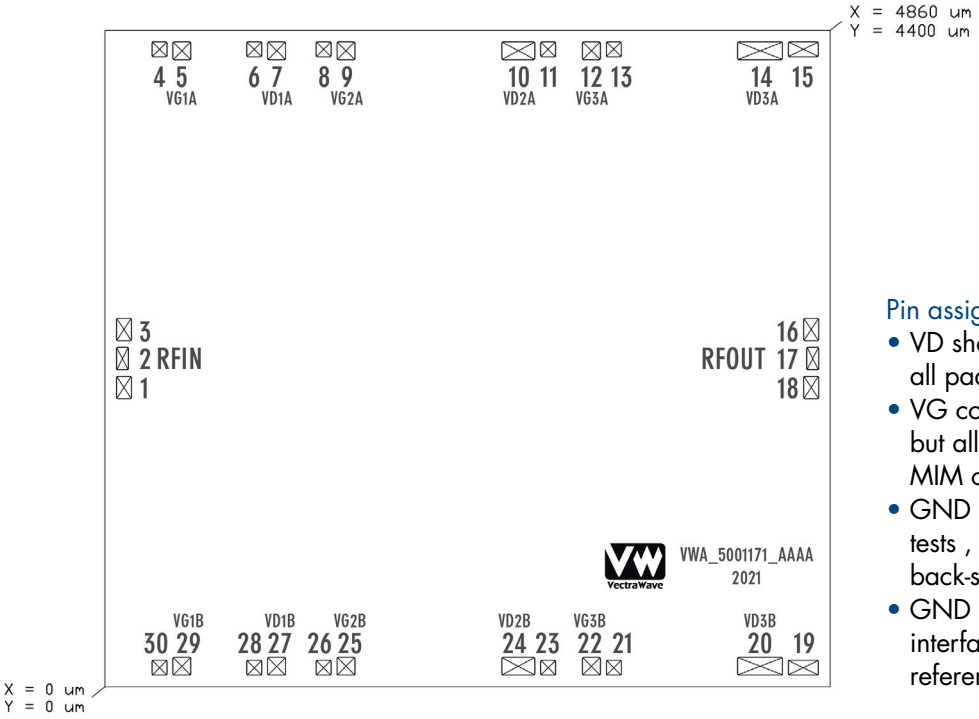
Power Gain (dB)



Supply curent - IDD (A)



Die Layout & Pin Out



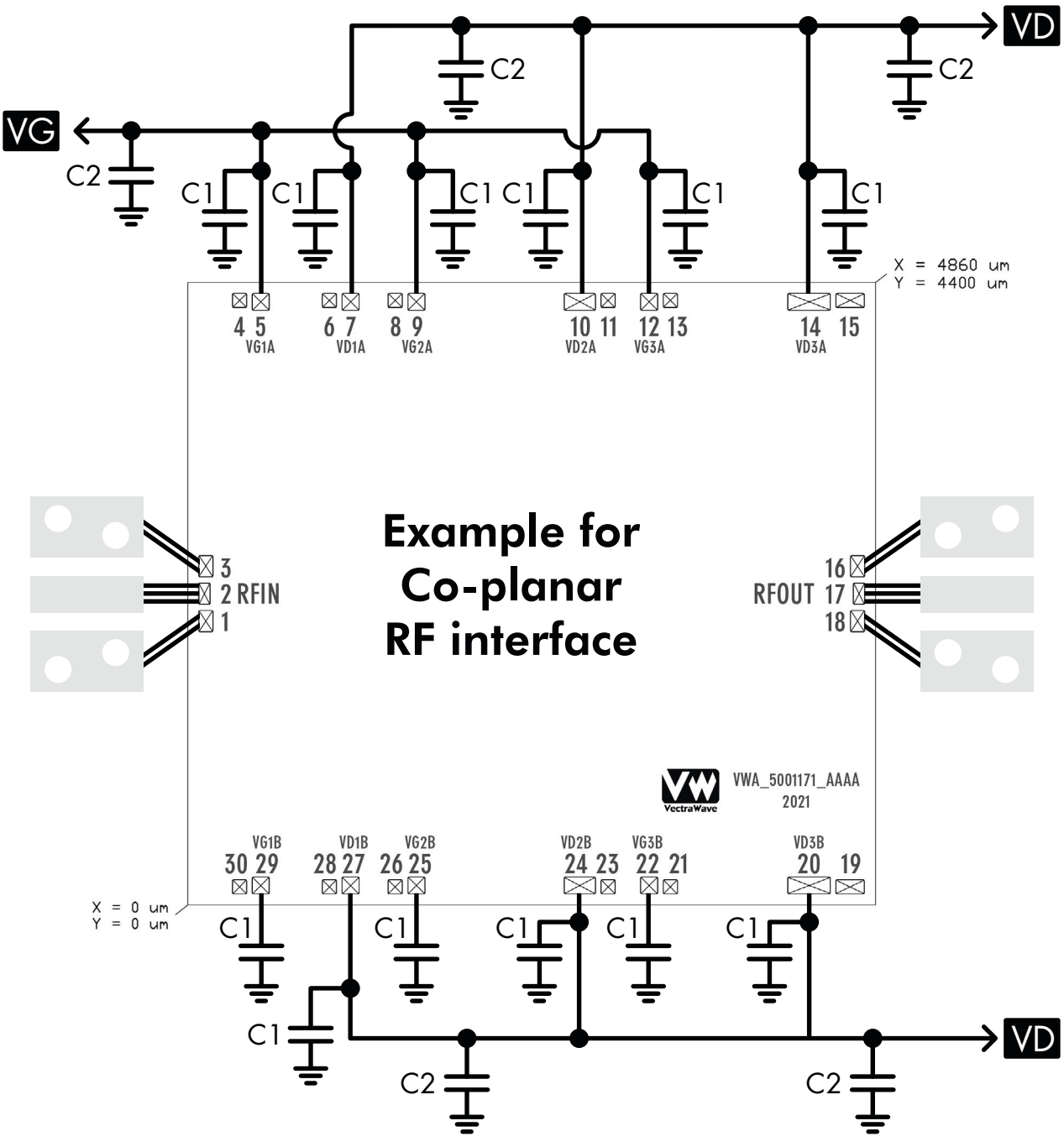
Pin assignments, NOTA :

- VD should be connected on both sides and all pads (VD1A/B , VD2A/B , VD3A/B)
- VG could be connected only on one side but all VG pads should be decoupled with MIM capacitor
- GND DC pads are mostly for on-wafer tests , for board decouplings GND from back-side is mor convenient to use
- GND RF pads could be used for coplanar interface (optional, micro-strip interface referenced to back-side is also possible)

Pad number	Pad center		Size (µm x µm)	Function		
	X (µm)	Y (µm)		Name	Value	Function
1	127	2006	100 x 150	Gnd		
2	117	2200	80 x 150	RFin	RF in	RF Input
3	127	2394	100 x 150	Gnd		
4	365	4273	100 x 100	Gnd		
5	515	4263	120 x 120	VG1A		Gate Bias
6	1000	4273	100 x 100	Gnd		
7	1150	4263	120 x 120	VD1A		Drain Bias
8	1465	4273	100 x 100	Gnd		
9	1615	4263	120 x 120	VG2A		Gate Bias
10	2770	4263	220 x 120	VD2A		Drain Bias
11	2970	4273	100 x 100	Gnd		
12	3260	4263	120 x 120	VG3A		Gate Bias
13	3410	4273	100 x 100	Gnd		
14	4390	4263	300 x 120	VD3A		Drain Bias
15	4680	4273	200 x 100	Gnd		
16	4733	2006	100 x 150	Gnd		
17	4743	2200	80 x 150	RFout	RF out	RF Output
18	4733	2394	100 x 150	Gnd		
19	4680	127	200 x 100	Gnd		
20	4390	137	300 x 120	VD3B		Drain Bias
21	3410	127	100 x 100	Gnd		
22	3260	137	120 x 120	VG3B		Gate Bias
23	1970	127	100 x 100	Gnd		
24	2770	137	220 x 120	VD2B		Drain Bias
25	1615	137	120 x 120	VG2B		Gate Bias
26	1465	127	100 x 100	Gnd		
27	1150	137	120 x 120	VD1B		Drain Bias
28	1000	127	100 x 100	Gnd		
29	515	137	120 x 120	VG1B		Gate Bias
30	365	127	100 x 100	Gnd		

Application circuit

- C1 = 100 pF MIM capacitor (dose to the die)
- C2 = 100 nF SMD capacitor (0402)



Bias-up procedure

1. Apply VG = -3V
2. Apply VD = +22V
3. Adjust VG to obtain I_{DQ} = 2.4A
4. Apply RF signal

Bias-down procedure

1. Turn OFF RF signal
2. Decrease VG to -3V
3. Decrease VD to 0V
4. Increase VG to 0V

Ordering Information

Product Code	Definition
VWA 5001171 AA	33 to 36GHz – 20W GaN/SiC Power Amplifier in die form

Associated Material

Product Code	Definition
Die Evaluation Board (die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder
and limit exposure to temperature
above 300 °C TO 3-4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/
EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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