

General Description

The **VWA5001201AA** is a Microwave Monolithic Integrated Circuit (MMIC) designed in HEMT (High Electron Mobility Transistor) structure for operating frequency range from 8 to 12GHz.

The MMIC is developed on a 250nm GaN/SiC process and is internally matched for 50Ω RF accesses.

It provides an output power of 5W, and associated Power Added Efficiency of 42%.

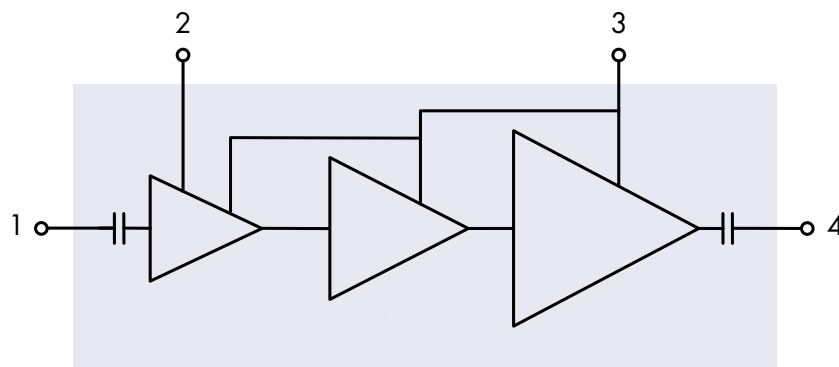
Features

- Operating frequency range: 8 to 12GHz
- Output Power: 38dBm @Pin = 14dBm
- PAE: 42% @Pin = 14dBm
- Linear Gain: 30dB
- DC bias: $V_D = +25V$, $I_{DQ} = 110mA$, $V_G = -2.5V$ (Typical)
- Chip size: QFN (6X6 mm)

Applications

- Driver
- Instrumentations
- Telecommunications

Functional Block Diagram & Pins Assignment



| Function | Pin number |
|----------|------------|
| RF in | 1 |
| VG | 2 |
| VD | 3 |
| RF out | 4 |

Electrical Specifications

Test conditions unless otherwise noted:

- IDQ = 110mA
- Simulation
- VD = 25V
- VG = -2.5V Typical
- Tamb = +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---|-----|-----|-----|-------|
| F | Frequency range | 8 | | 12 | GHz |
| BW | Operating Bandwidth | | 4 | | GHz |
| G | Small signal gain | | 30 | | dB |
| S11 | Input Return loss | | -10 | | dB |
| S22 | Output Return loss | | -10 | | dB |
| POUT | Output power (Pin=14dBm) | | 38 | | dBm |
| PAE | Power Added Efficiency (Pin=14dBm) | | 42 | | % |
| ID | Drain current (Pin=14dBm) | | 0.9 | | A |
| VD | Drain voltage | | 25 | | V |
| P1dB | P1dB compression | | NA | | A |
| ΔG | Small signal gain temperature coefficient | | NA | | dB/°C |

Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|--------|-------------------------|-------|------|
| VD | Quiescent drain voltage | 25 | V |
| IDQ | Quiescent drain current | 110 | mA |
| VG | Quiescent gate voltage | -2.5 | V |

Absolute Maximum Ratings

| Symbol | Maximum Ratings | Min | Unit |
|--------|--|-----------|------|
| VD | Drain voltage | 35 | V |
| ID | Maximum saturated drain current | 0.5 | A |
| VG | Gain voltage | -10 to -2 | V |
| PDISS | Power dissipated (Tcarrier=85°C) mean in pulsed mode | NA | W |
| PIN | Maximum input power | 25 | dBm |
| Tj | Junction temperature | 225 | °C |
| Ta | Operating temperature | -40/+85 | °C |
| Tstg | Storage temperature | -55/+150 | °C |

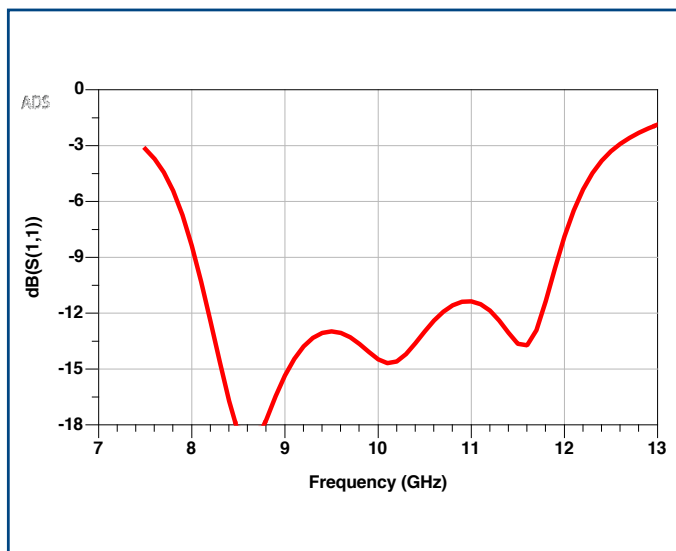
Operation of this device above any of these parameters may cause permanent damage.

Typical performances (Small signal / simulation)

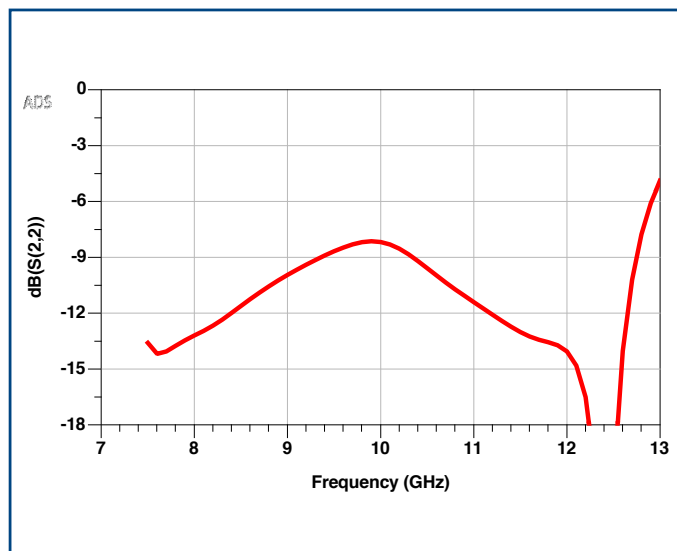
Simulated conditions unless otherwise noted:

- $V_D = 25V$
- $I_{DQ} = 110mA$
- $P_{in} = -20dBm$
- $T_{amb} = +25^{\circ}C$

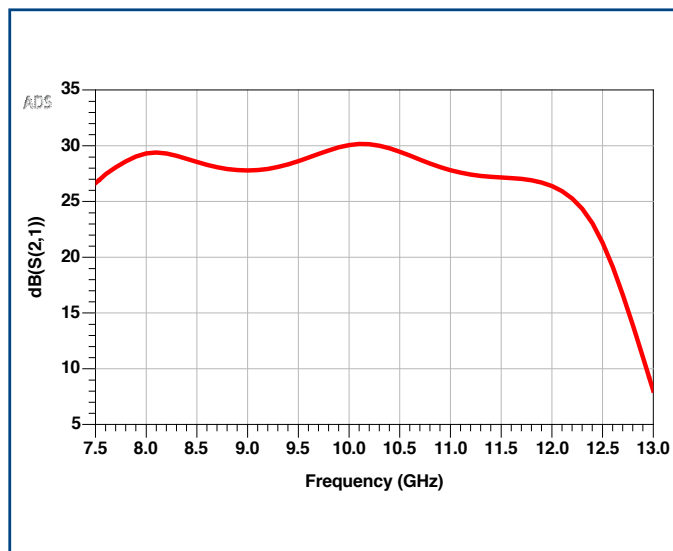
Input return loss (S11)



Output return loss (S22)



Small signal gain (S21)

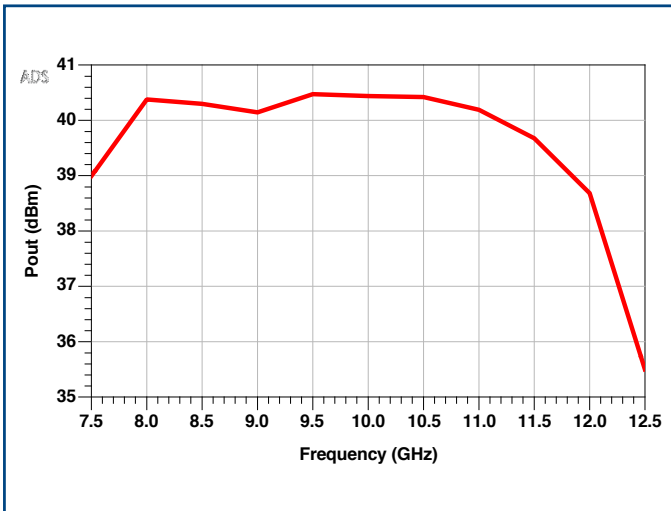


Typical performances (Large signal / simulation)

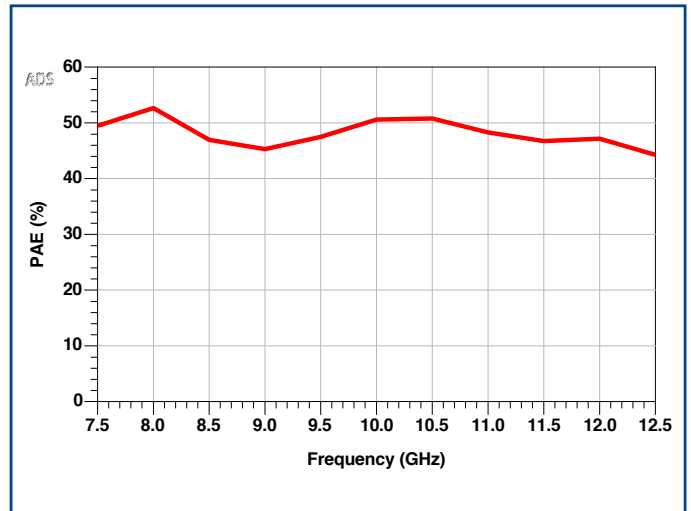
Simulated conditions unless otherwise noted:

- $V_D = 25V$
- $I_{DQ} = 110mA$
- $P_{in} = 14dBm$
- $T_{amb} = +25^{\circ}C$

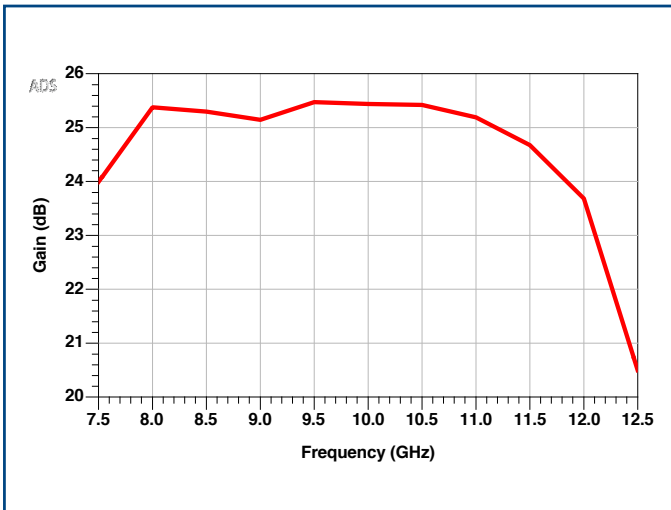
Output power vs frequency



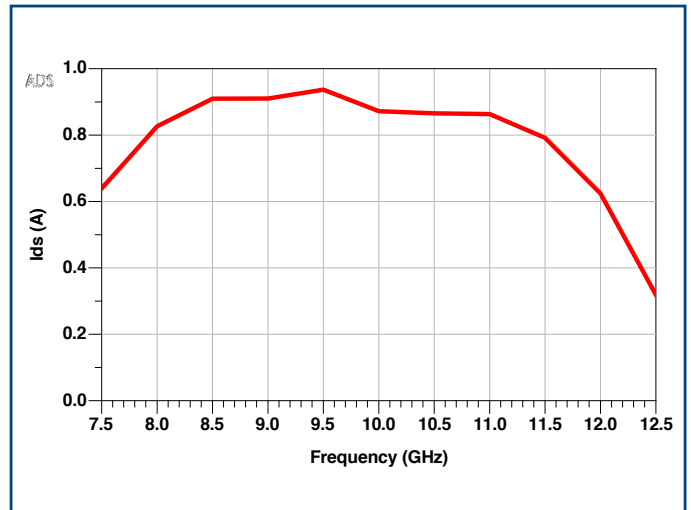
PAE vs frequency



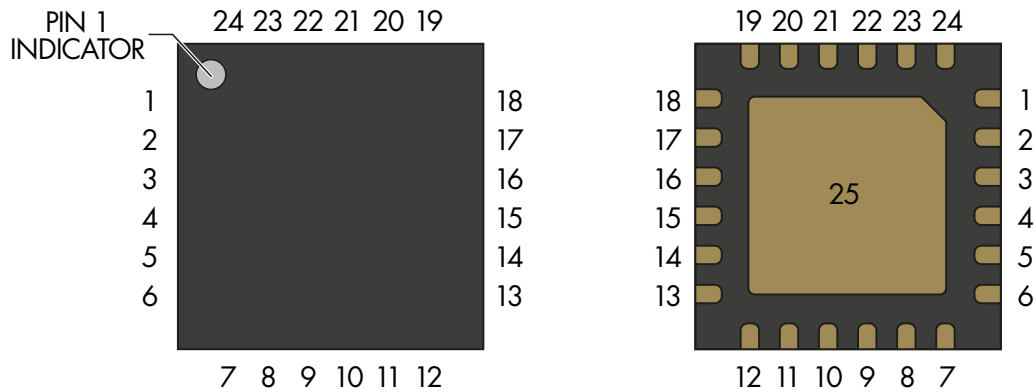
Power gain vs frequency



Drain current vs frequency

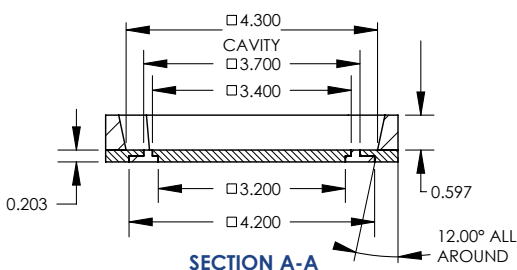
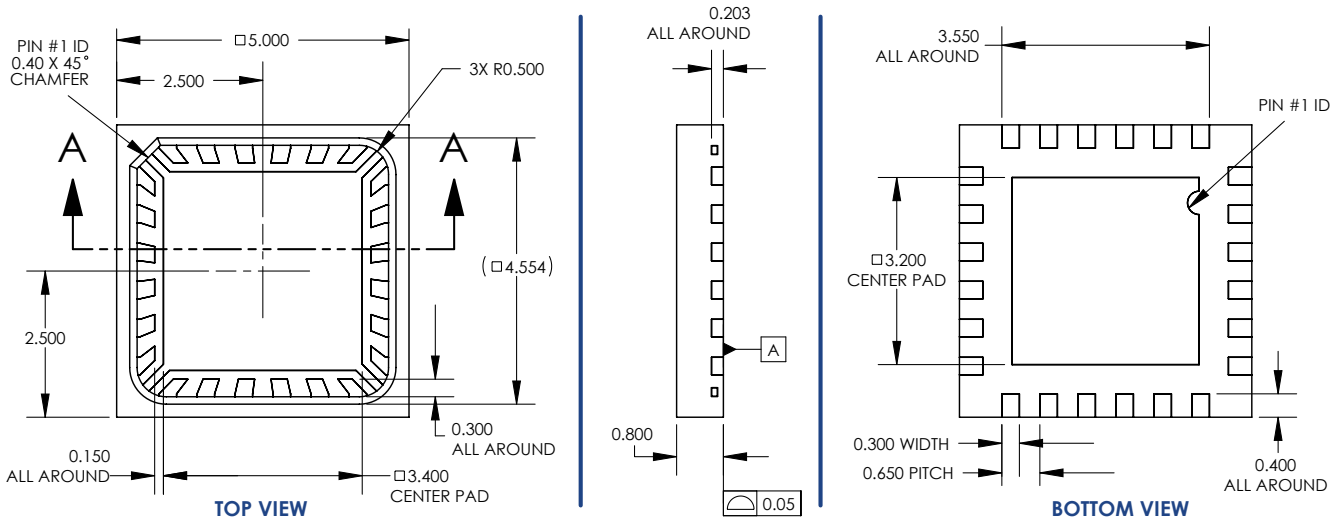


Pin Layout & Pin Description



| Pin number | Symbol | Description |
|-----------------------------|--------|--|
| 1,2,4 - 15,17 - 19,21,22,24 | NC | No connection inside of package |
| 3 | RF IN | RF input. 50Ω |
| 16 | RF OUT | RF output. 50Ω |
| 20 | VD | Drain voltage. Bypass network required |
| 23 | VG | Gate voltage. Bypass network required |
| 25 | GND | Center paddle ground |

Mechanical Plan



- Notes**
- Materials: Lead frame: copper 194fh, thk = 0.203 0.008
Body: semiconductor molding epoxy, contact quik-pak for details.
 - Finish: Lead frame: electroless nickel per mil-c-26074, class 1, 200 to 300 microinches (2.5um-7.6um) thick. Gold plate per mil-g-45204, type 3, grade a, class 1 (40 To 80 microinches (1um-2um) thick).
Body surface finish: vdi 21-24 (1.12-1.6 Ra)
 - Package mismatch: body offset for lead frame = 0.076mm max.
 - Unless otherwise specified, radius on all molded edges and corners = 0.25mm max.
 - Package conforms to jedec mo-220

Ordering Information

| Product Code | Definition |
|----------------|---|
| VWA 5001201 AA | 8 to 12GHz - 5W GaN/SiC Power Amplifier 5x5 QFN |

Associated Material

| Product Code | Definition |
|--|-----------------|
| Packaged die | Contact factory |
| Die Evaluation Board (die EVB) | Contact factory |
| Packaged die Evaluation Board (packaged die EVB) | Contact factory |
| Mechanical files (DXF) | Contact factory |
| Measurements files (S2P) | Contact factory |

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3-4 minutes, maximum

ESD Sensitivity Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114



CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
• Halogen Free (Chlorine, Bromine)
• Antimony Free
• TBBP-A (C15H12Br4O2) Free
• PFOS Free
• SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave:

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Represented by