27 to 32GHz,1.3dB NF, 26dB Low Noise Amplifier

DATA SHEET PRELIMINARY VM205D

General Description

The VM205D is 3 stage Low-Noise amplifier MMIC operating in the frequency range 27 to 32 GHz.
The device has a linear gain of 26 dB and a typical noise figure of 1.3 dB. Output RF power is 19 dBm for a biasing current of 78 mA at +3.5V supply voltage.
It is manufactured with a 100nm pHEMT GaAs process and is especially suited for radar and for telecommunication applications.

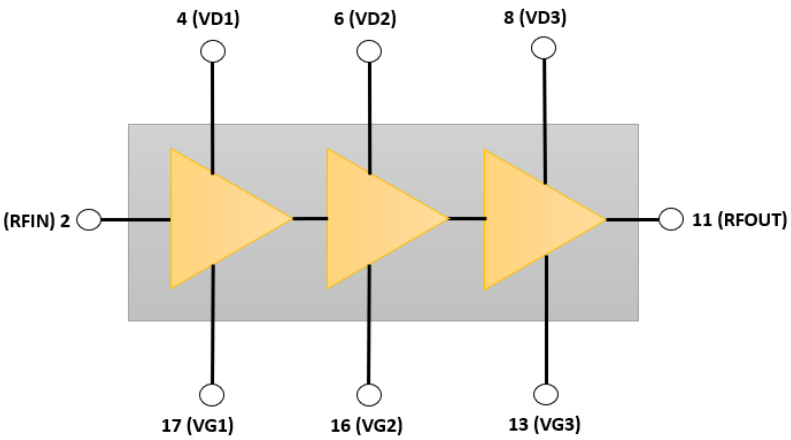
Typical Features

- Operating frequency range: 27 to 32 GHz
- Gain: 26 dB
- Noise figure: 1.3 dB
- P1dB = 19dBm - Psat= 21dBm
- Gain Flatness: +/- 1 dB
- Input Return Loss: -10 dB typ.
- Output Return Loss: -10 dB typ.
- Power supply: 78 mA @ V_D=+3.5 V, V_G=-0.58V typ.
- Die Size: 1.2 x 2.4 x 0.1 (mm)

Applications

- Radar
- Test and Measurement
- Telecommunications

Functional Block Diagram and Pin Assignment



Function	Pin Number
RFIN	2
V_{D1}	4
V_{D2}	6
V_{D3}	8
RFOUT	11
V_{G3}	13
V_{G2}	16
V_{G1}	17

Electrical Specifications

Operating conditions unless otherwise noted:

- $V_D=V_{D1}=V_{D2}=V_{D3}$=+3.5V
- $V_G=V_{G1}=V_{G2}=V_{G3}$=-0.58V
- $I_D=I_{D1}+I_{D2}+I_{D3}$=78mA
- Tamb.= 25 ° C

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	27		32	GHz
G	Linear gain		26		dB
P1dB	Output power at 1dB gain compression		19		dBm
Psat	Output saturated power		21		dBm
NF	Noise Figure		1.3		dB
PAE	Power Added Efficiency		28		%
S11	Input Return loss		-10		dB
S22	Output Return loss		-10		dB
$V_{D1\_2\_3}$	Operating supply voltage		+3.5		V
I_D	Supply current		78		mA
$V_{G1\_2\_3}$	Gate voltage	-0.6	-0.58	-0.4	V

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_D	Drain voltage		+8	V
I_D	Supply Current	0	190	mA
V_G	Gate Voltage	-2	0	V
Pin	CW Input Power		+10	dBm
Tst	Storage temperature	-55	+125	°C
Top	Operating temperature	-40	+85	°C
Tch	Channel temperature		+150	°C

Operation of this device above any of these parameters may cause permanent damage.

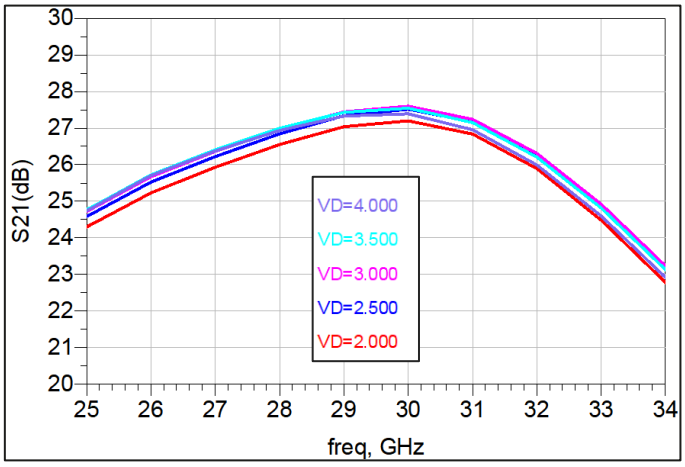
Typical Performance (Post-layout Simulations)

Small signal performances Versus Drain Voltage

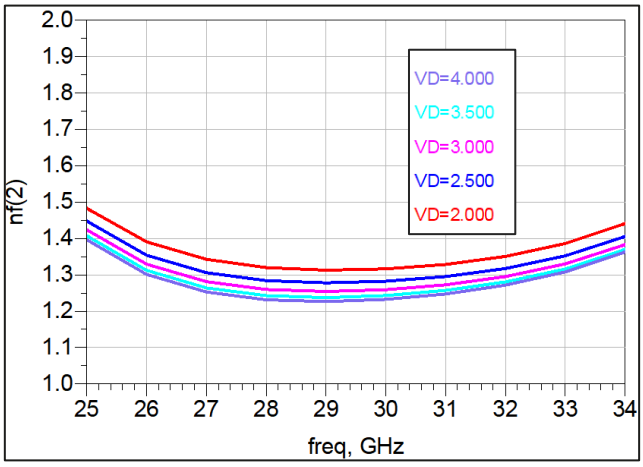
Simulation conditions unless otherwise noted:

- $V_D=V_{D1}=V_{D2}=V_{D3}=+3.5V$
- $V_G=V_{G1}=V_{G2}=V_{G3}=-0.58V$
- $I_D=I_{D1}+I_{D2}+I_{D3}=78mA$
- Tamb.= 25 ° C

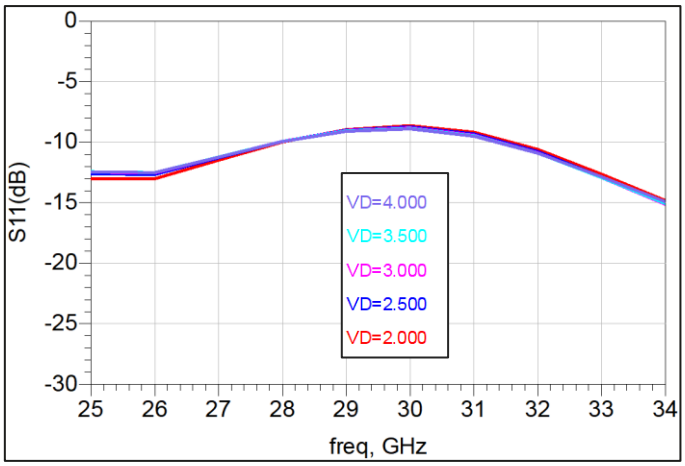
Small Signal Gain(dB)



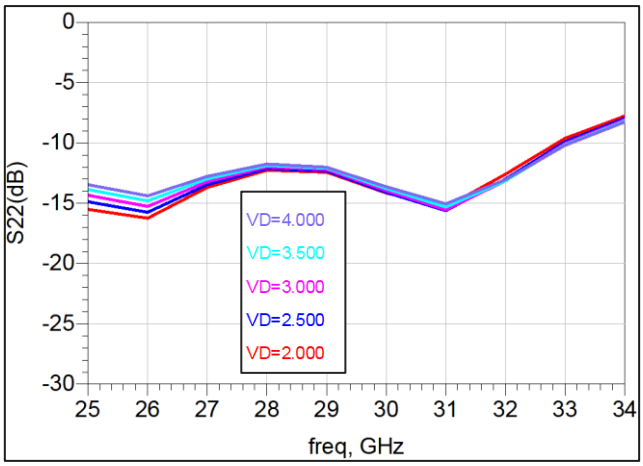
Noise Figure(dB)



Input Return Loss(dB)



Output Return Loss(dB)



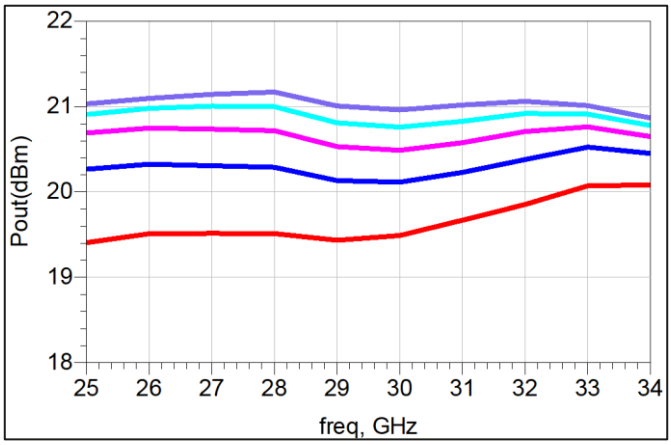
Typical Performance (Post-layout Simulations)

Large signal performances Versus Gain Compression Level

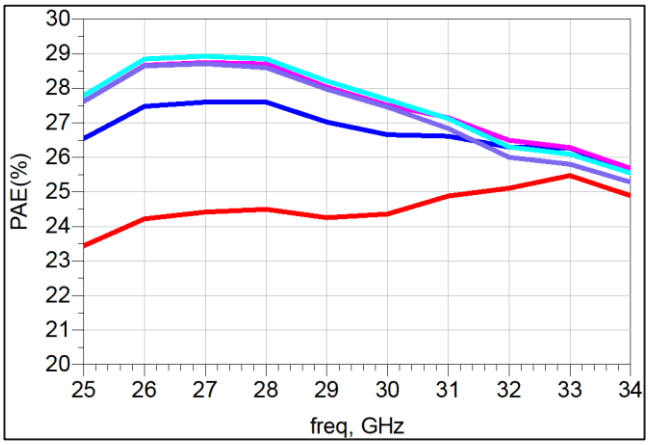
Simulation conditions unless otherwise noted:

- $V_D=V_{D1}=V_{D2}=V_{D3}=+3.5V$
- $V_G=V_{G1}=V_{G2}=V_{G3}=-0.58V$
- $I_D=I_{D1}+I_{D2}+I_{D3}=78mA$
- Tamb.= 25 ° C

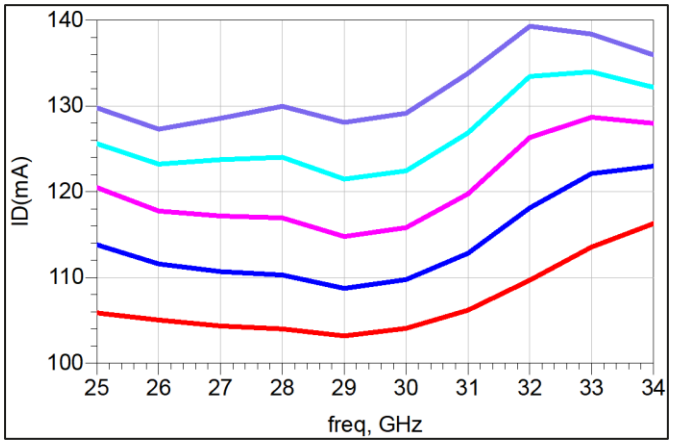
Output Power(dBm)



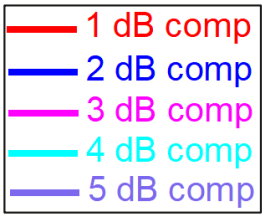
Power Added Efficiency(%)



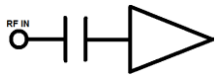
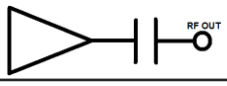
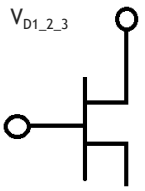
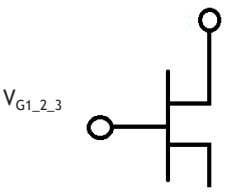
Drain Current(mA)



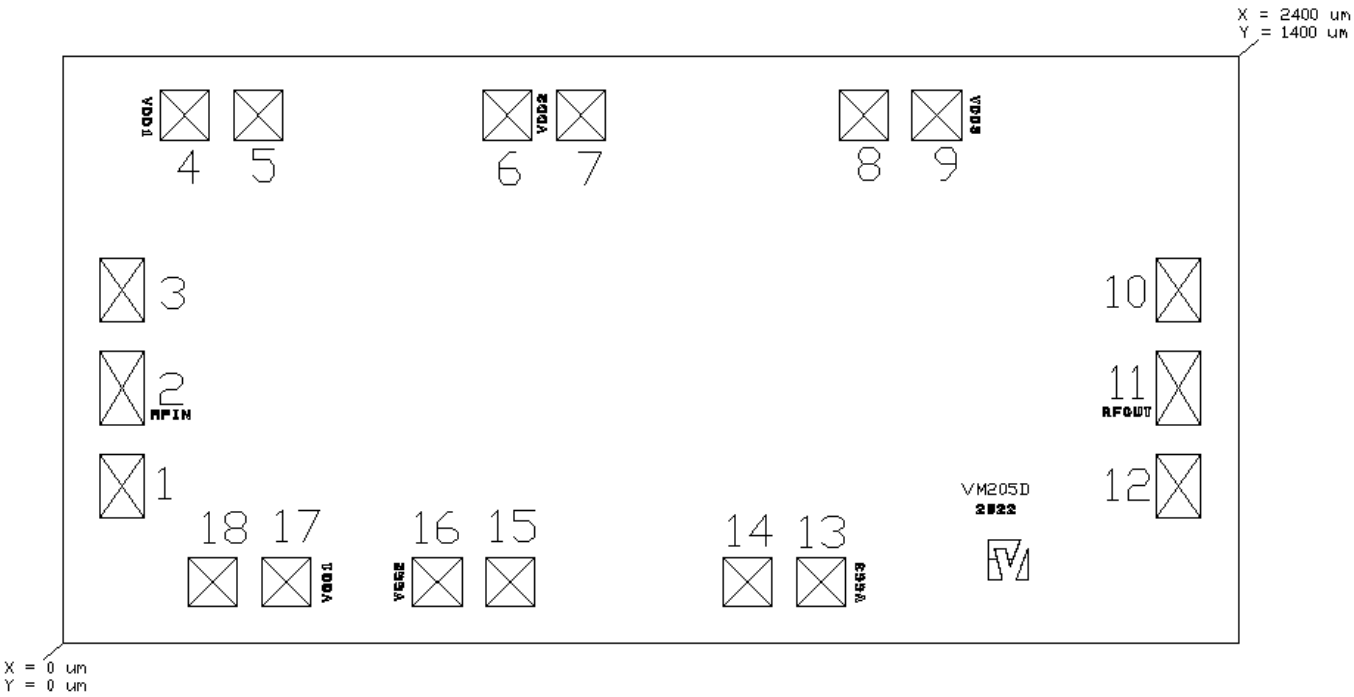
Gain Compression levels



Pin Description

Pin number	Name	Description	Electrical interface
2	RFIN	AC coupled, amplifier input access. Internally matched 50 Ohms.	
11	RFOUT	AC coupled amplifier output access. Internally matched 50 Ohms.	
4, 6, 9	V_{D1}, V_{D2}, V_{D3}	1st, 2nd and 3rd stage drain biasing access	
17, 16, 13	V_{G1}, V_{G2}, V_{G3}	1st, 2nd and 3rd stage gate biasing access	
Die Bottom	GND	Die Bottom must be connected to RF and DC Ground	

Die Layout



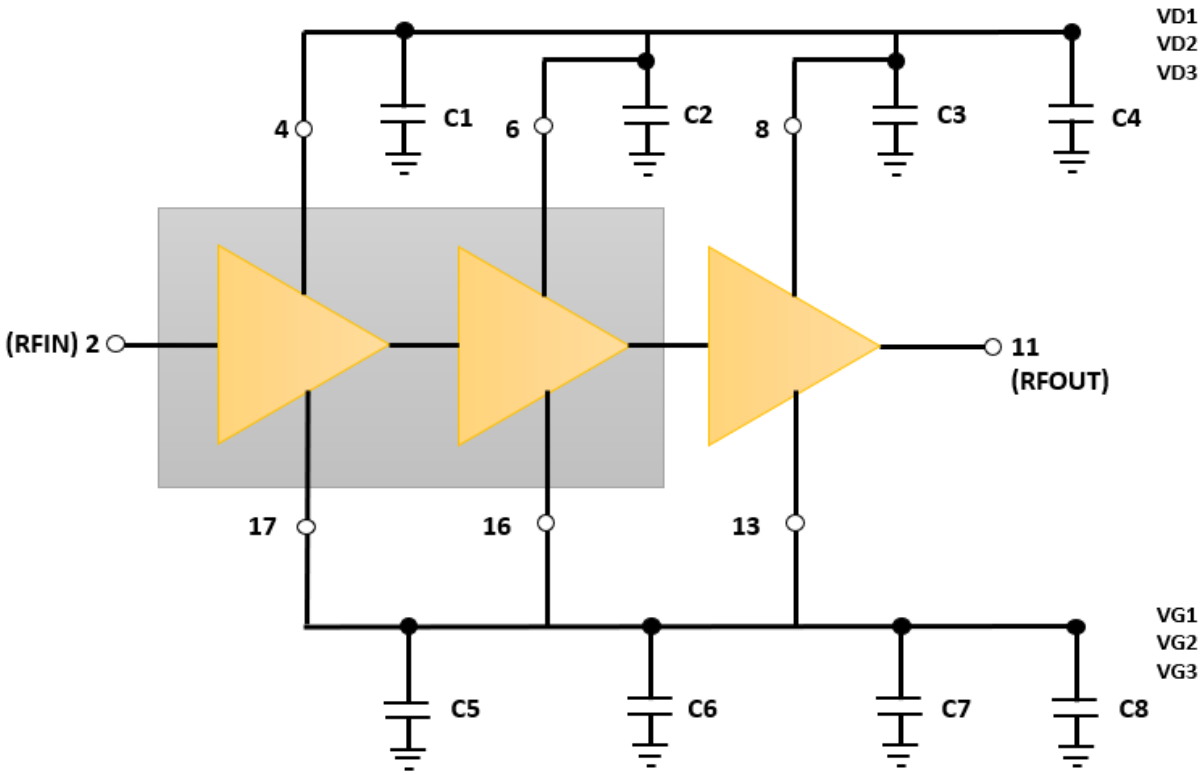
Die Pin Out

Pad Number	Pad center		Size	Description		
	x(μm)	y(μm)	μm×μm	Name	Value	Function
1	119	322	90x130	Gnd		
2	119	522	90x150	RFin	RF in	RF Input
3	119	722	90x130	Gnd		
4	247	1078	100x100	VDD1		Drain Bias
5	397	1078	100x100	GND		
6	905	1078	100x100	GND		
7	1055	1078	100x100	VDD2		Drain Bias
8	1633	1078	100x100	GND		
9	1783	1078	100x100	VDD3		Drain Bias
10	2276	722	90x130	GND		
11	2276	522	90x150	RFout	RF out	
12	2276	322	90x130	GND		
13	1547	126	100x100	VGG3		Gate Bias
14	1397	126	100x100	GND		
15	913	126	100x100	GND		
16	763	126	100x100	VGG2		Gate Bias
17	454	126	100x100	VGG1		Gate Bias
18	304	126	100x100	GND		

Application Circuit

- C1, C2, C3, C5, C6, C7 = 100 pF MIM Capacitor (close to the die)
- C4 &C8 = 1 µF

RF In and RF Out: 1 Gold Wire (25µm diameter Au)



Bias-up procedure

1. Set V_{G1}, V_{G2} and V_{G3} to -1V,
2. Set V_{D1},V_{D2} and V_{D3} to +3.5V,
3. Increase V_{G1}, V_{G2} and V_{G3} to obtain I_D= 78 mA (V_G =-0.5V Typ.),
4. Turn ON RFIN

Bias-down procedure

1. Turn OFF RFIN
2. Decrease V_{G1}, V_{G2} and V_{G3} to -1V,
3. Decrease V_{D1},V_{D2} and V_{D3} to 0V,
4. Set V_{G1}, V_{G2} and V_{G3} to 0V .

Ordering Information

Product Code	Definition
VM205D	27 to 32 GHz ,1.3dB NF, 26dB Low Noise Amplifier in Die form

Associated Material

Product Code	Definition
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3-4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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