Vectrawave
RF & Millimeter Wave MMIC Design

1 to 20GHz - 16dB - 27dBm
Medium Power Amplifier

VM056D

General Description

The VM056D is a medium power amplifier designed on a 0.15µm pHEMT GaAs process. The device delivers more than +27dBm of output power at saturation regime, and provides more than 15dB of gain from 1 to 20GHz with less than 1dB of flatness with an excellent group delay between 6-18GHz in typical application.

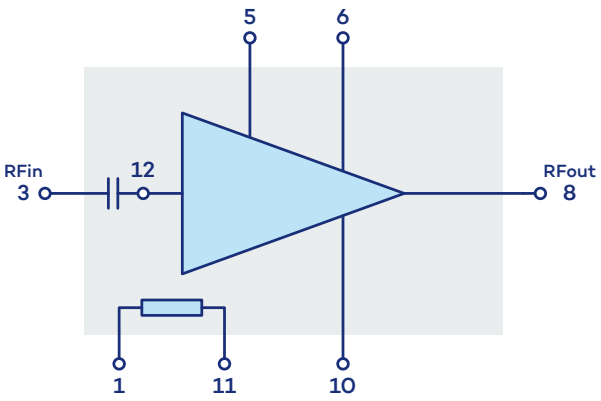
Features

Wide band	**1 – 20GHz**
Flat group delay	
50ΩRF Single ended RF input and output	
AC coupled in, DC coupled out	
High output P_{SAT}	**>+27dBm**
Small signal gain	**16dB**
Power supply	**290mA @ +8V**
Chip size	**3 x 1.3 x 0.1 (mm)**

Applications

- Wide Band Low Noise Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	3
V_{G2}	5
V_{D_LOAD}	6
V_D & RF out	8
V_G	10
RA	1
RB	11
CA	12

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +8V
- V_{G2} = +3V
- I_{DD} = 290mA @-1V < V_G < 0V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	1		20	GHz
G	Small signal gain	15	16		dB
ΔG	Small signal gain flatness		+/-1		dB
NF	Noise figure (@10GHz)			3.5	dB
TOI	Simulated TOI		30		dBm
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
P1dB	Output P1dB		24		dBm
P_{SAT}	Saturated output power		27		dBm
I_D	Supply current		290		mA

Environmental parameters

Symbol	Parameter	Min	Max	Unit
Top	Operating temperature range	-40	+85	°C
Tstg	Storage temperature range	-55	+125	°C

Absolute Maximum Ratings

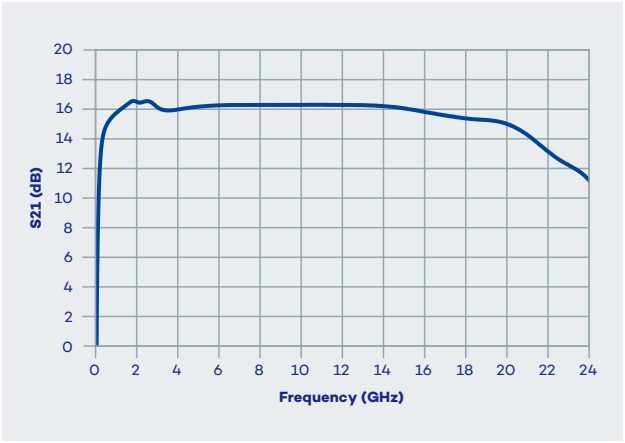
Symbol	Parameter	Min	Max	Unit
V_D	Positive External DC bias voltage		9	V
V_{G1}	Gate voltage first stage	-2.5		V
V_{G2}	Gate control input access for second stage	-1	V_D/2	V
Pin max	RF input power (In)		18	dBm
Pdiss (CW)	Continuous power dissipation (@85°)		3.3	W

Operation of this device above any of these parameters may cause permanent damage.

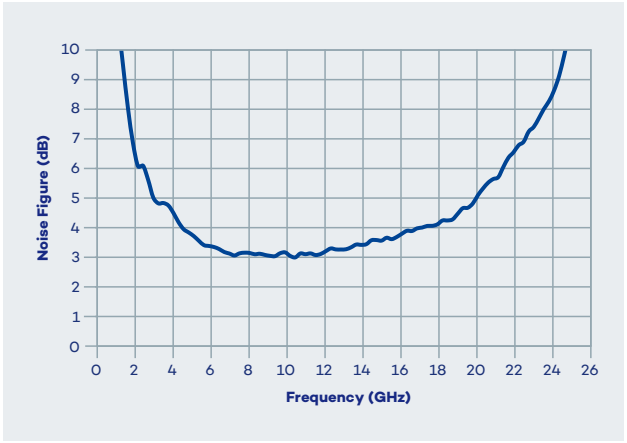
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- I_D = 290mA
- V_D = +8V
- V_{G2} = +3V
- I_{DD} = 290mA @-1V < V_G < 0V

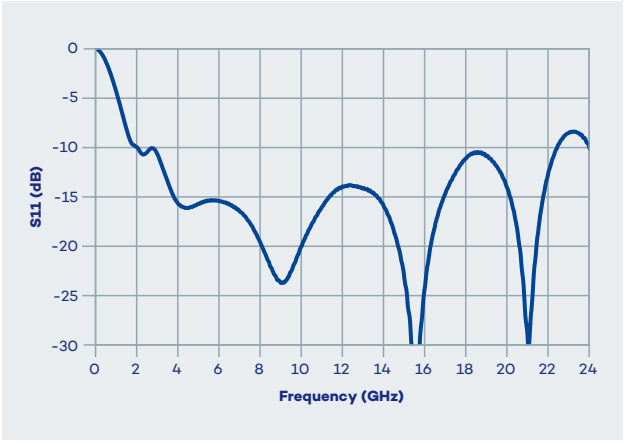
Small Signal Gain vs Frequency



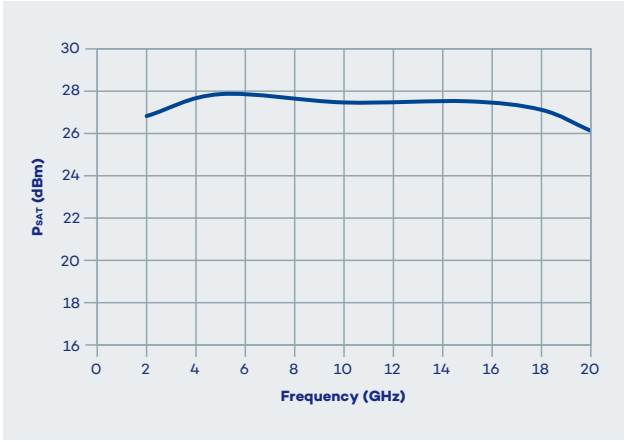
Noise Figure vs Frequency



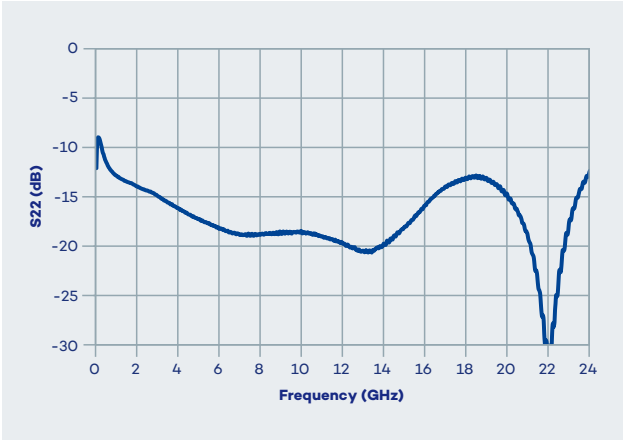
Input Return Loss vs Frequency



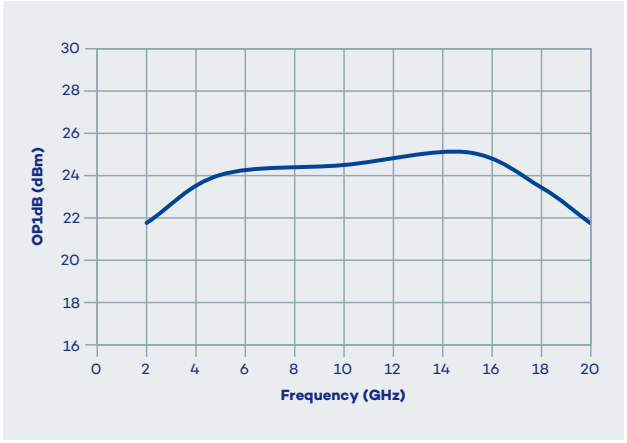
Saturated Output Power vs Frequency



Output Return Loss vs Frequency



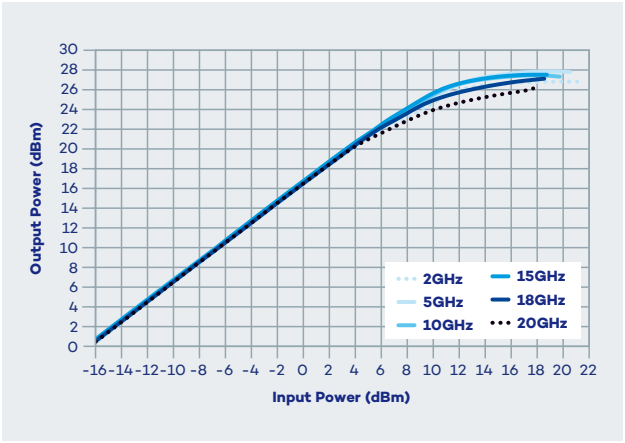
Output P1dB vs Frequency



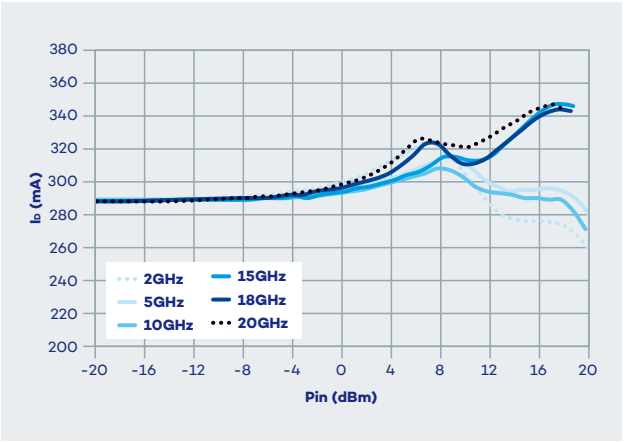
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- I_D = 290mA
- V_D = +8V
- V_{G2} = +3V
- I_{DD} = 290mA @-1V < V_G < 0V

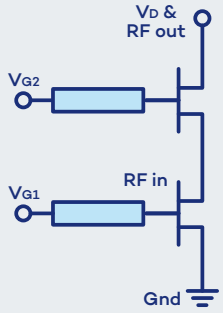
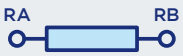
Output Power vs Input Power for various Frequency



Drain Current vs Input Power for various Frequency



Access description

Pin number	Name	Description	Electrical interface
3	RF in	RF Amplifier input, this access is AC coupled and internally matched to 50Ω.	
5	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +3V for nominal biasing conditions.	
6	V_{D_LOAD}	Drain termination load decoupling access. For lower frequency appli-cations, this access can be connec-ted to a MIM 100pF or 1000pF capacitor, with a low inductance connection.	
8	RF out	RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to feed the drain current (ID), by using a wide bandwidth external Bias-T structure.	
10	V_{G1}	Gate control input access for first stage distributed amplifier structure. Adjust VG1 to obtain the desired Drain current (~-0.2V for nominal biasing conditions)	
1	RA	Embedded resistor for low frequencies applications. Unused for nominal biasing conditions.	
11	RB	Embedded resistor for low frequencies applications. Unused for nominal biasing conditions.	
Die Bottom	Gnd	Die must be connected to HF and DC Ground	

Die Layout & Pin Out

- Die size = 3020µm x 1298µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	99	118	75 x 75	RA	
2	99	250	75 x 75	Gnd	
3	99	400	75 x 75	RFin	RF Input
4	99	549	75 x 75	Gnd	
5	111	787	80 x 100	V_{G2}	Gate Bias
6	137	1202	150 x 100	V_{D_LOAD}	
7	2922	1215	75 x 75	Gnd	
8	2922	1065	75 x 75	RFout	RF Output
9	2922	915	75 x 75	Gnd	
10	2909	294	100 x 150	V_{G1}	Gate Bias
11	292	118	75 x 75	RB	
12	371	400	75 x 75	CA	

- Die bottom must be connected to ground (RF and DC)

Bias-up procedure

1. Apply V_{G1} = -1V
2. Apply V_D = +8V
3. Apply V_{G2} = +3V
4. Increase V_{G1} to obtain I_D = 290mA (typically V_G = -0.2V)
5. Apply RF signal

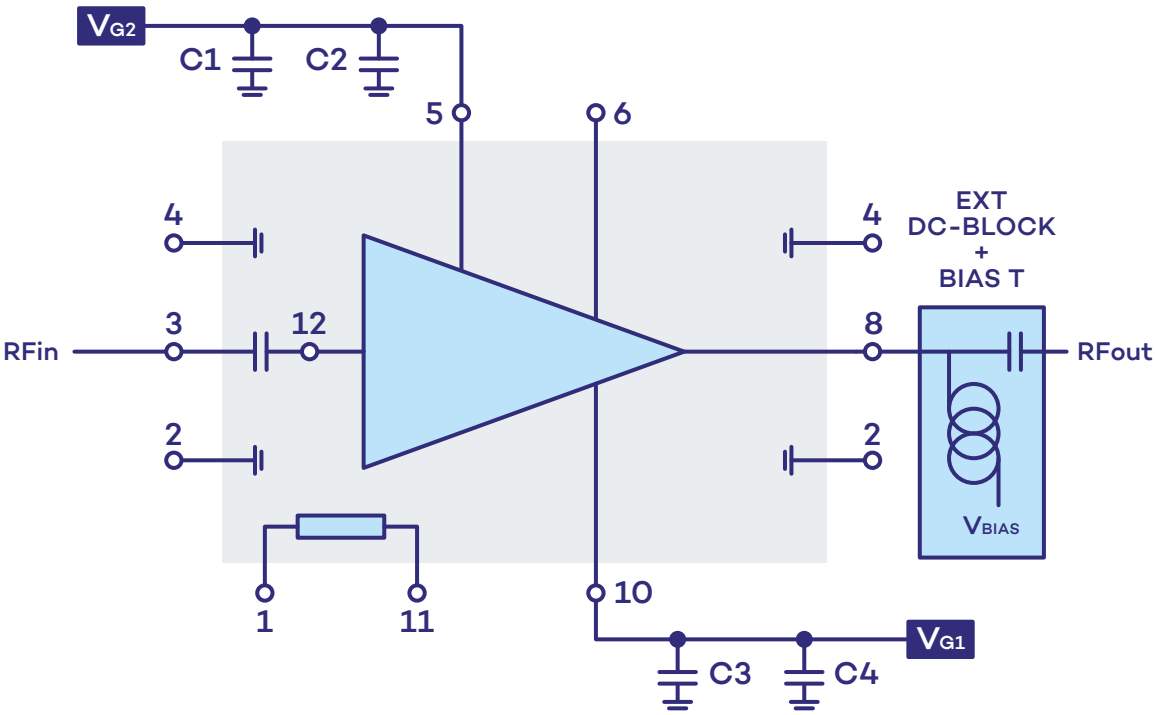
- Always apply V_{G1} before applying V_D
- This stress may cause permanent damage on component.

Bias-down procedure

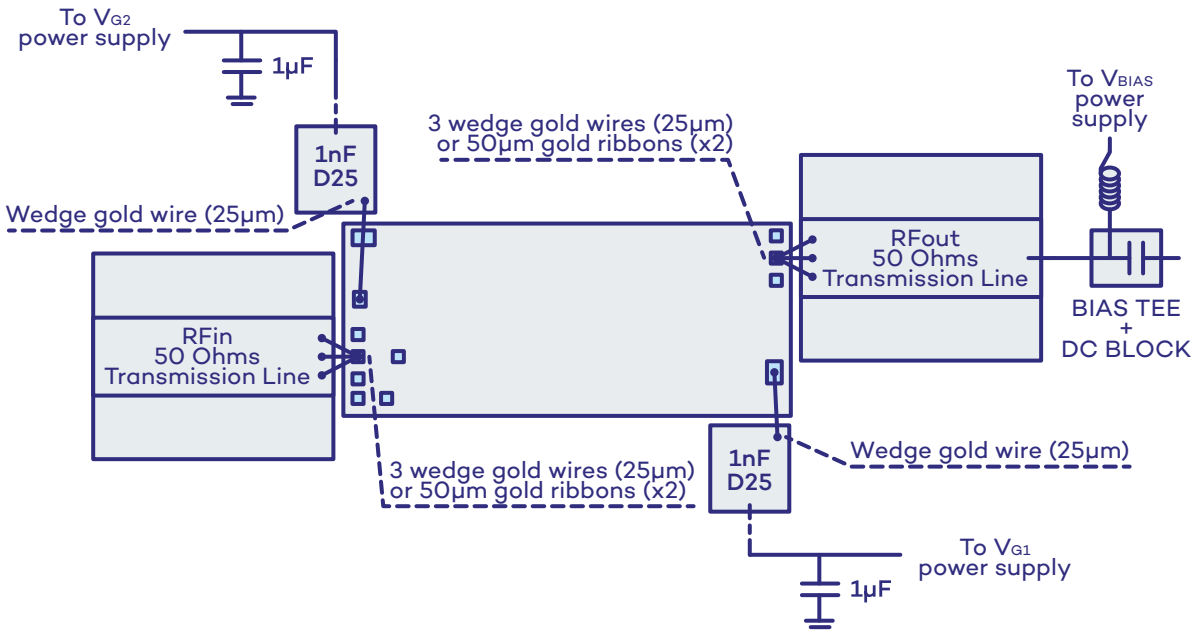
1. Turn off RF signal
2. Decrease V_{G1} to -1V
3. Set V_{G2} to 0V
4. Set V_D to 0V
5. Set V_{G1} to 0V

Application circuit

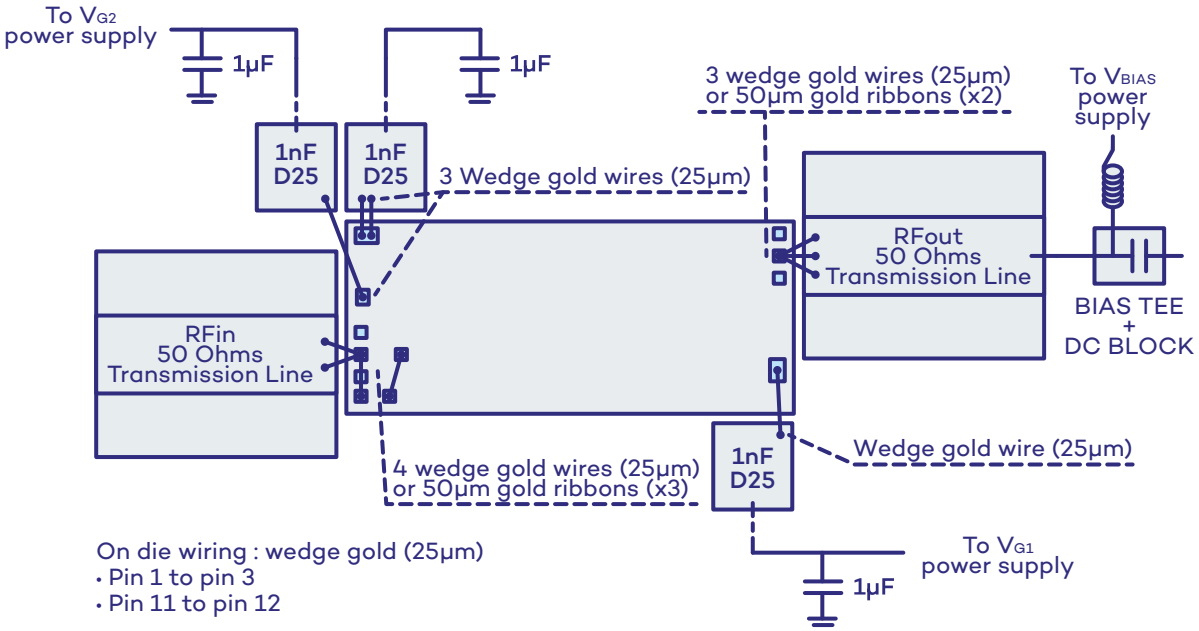
- C1 and C4 = 1µF
- C2 and C3 = 1nF capacitors are MIM type and must be placed as close as possible to the die access.



Typical Application



Low Frequency Application



On die wiring : wedge gold (25µm)
- Pin 1 to pin 3
- Pin 11 to pin 12

Ordering information

Product Code	Parameter
VM056D	1 to 20GHz - 16dB - 27dBm Medium Power Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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