Vectrawave
RF & Millimeter Wave MMIC Design

8 to 12Ghz - 19dB - 1.0dB NF
Single bias Low Noise Amplifier

VM134D

General Description

The VM134D is a low noise amplifier MMIC operating in the frequency range 8 to 12GHz.

The device has a linear gain of 19dB and a typical noise figure of 1.0dB. Typical operating supply current is only 30mA with a supply voltage at +3V.

It is manufactured on a PHEMT Technology and is especially suited for radar and telecommunication applications.

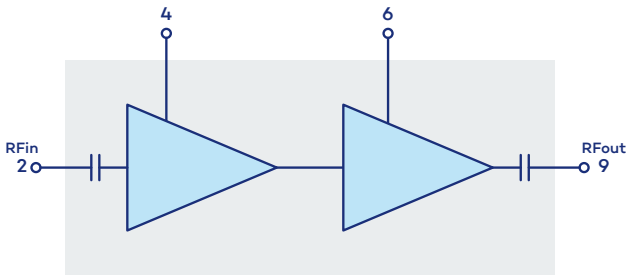
Features

Frequency range	**8 – 12GHz**
Gain	**19dB**
Noise Figure	**1.0dB**
Gain Flatness	**+/- 0.7dB**
Input Return Loss	**-10dB typ.**
Output Return Loss	**-12dB typ.**
Power supply	**30mA @+3V**
Chip size	**1.4 x 1.4 x 0.1 (mm)**

Applications

- Radar
- Test and measurement
- Telecommunications

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{DD1}	4
V_{DD2}	6
RF out	9

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- $I_{DD} = I_{DD1} + I_{DD2}$ = 30mA
- $V_{DD} = V_{DD1} = V_{DD2}$ = +3V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8		12	GHz
G	Linear gain		19		dB
ΔG	Small signal gain flatness		+/-0.7		dB
NF	Noise Figure		1.0		dB
OP1dB	Output power @1dB compression		7		dBm
P_{SAT}	Saturated Output Power		9		dBm
S11	Input return loss		-10		dB
S22	Output return loss		-12		dB
V_{DD1_2}	Operating supply voltage		+3		V
I_{DD}	Supply current		30		mA

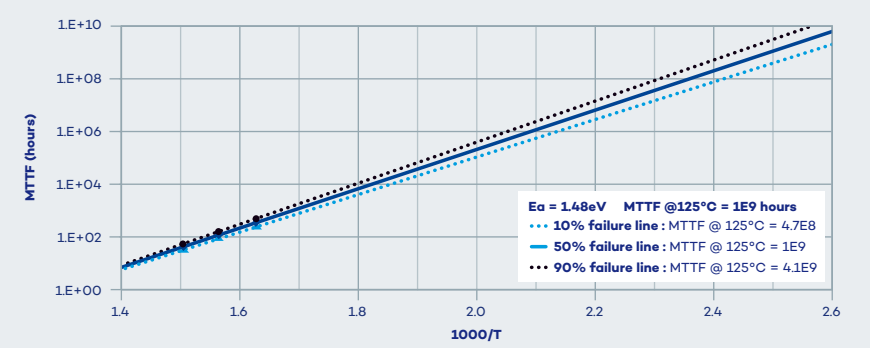
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD1_2}	Drain voltage		+4	V
Pin	CW input power		+10	dBm
V_G	Gate voltage		+10	dBm
Tst	Storage temperature	-55	+125	°C
Top	Operating temperature	-40	+85	°C
Tch	Channel temperature		+150	°C

Operation of this device above any of these parameters may cause permanent damage.

MTTF (Provided by Foundry)

0.15µm Low noise pHEMT (PL15-10) vs MTTF Test Arrhenius Plot

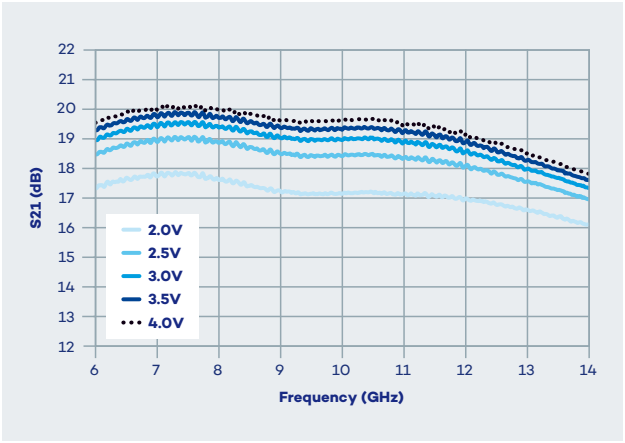


The values shown here are calculated, only to be used as a guideline and represent reliability information under Vds = +5V and drain current of 267mA/mm.

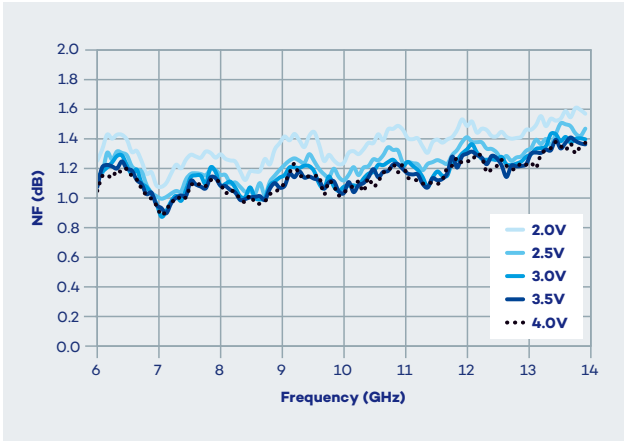
Typical Performance
(Board measurements)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- Typically, I_{DD} = 30mA @V_{DD} = +3V

Small Signal Gain vs V_{DD}

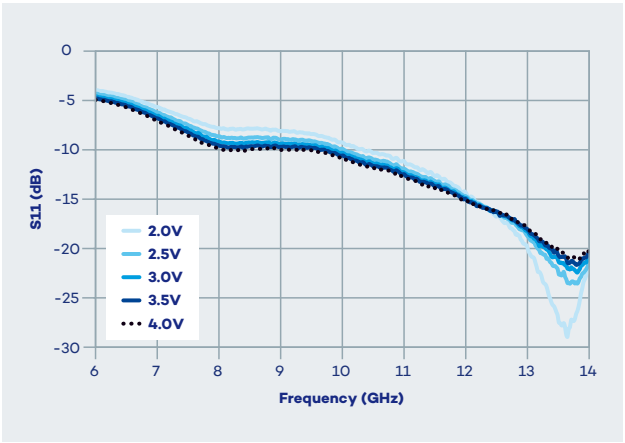


Noise Figure vs V_{DD}

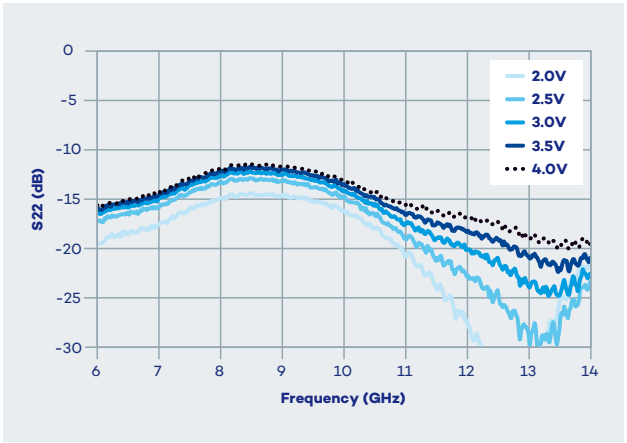


Measurement accuracy for Noise Figure is +/- 0.2dB.

Input Return Loss vs V_{DD}



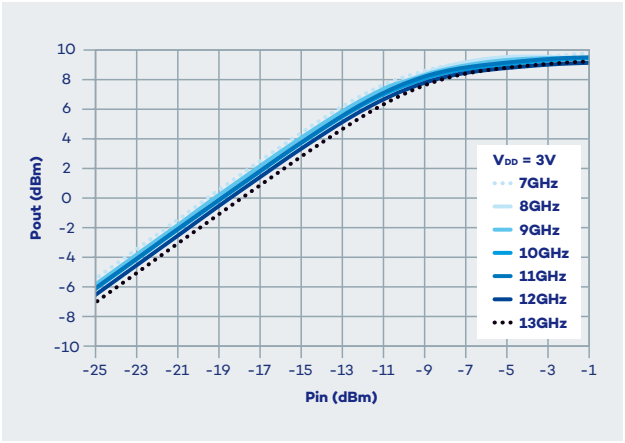
Output Return Loss vs V_{DD}



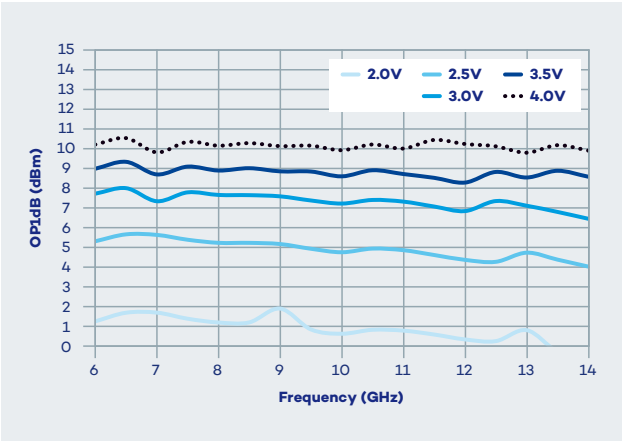
Typical Performance
(Board measurements)

Test conditions: unless otherwise noted
• T_{amb} = +25°C

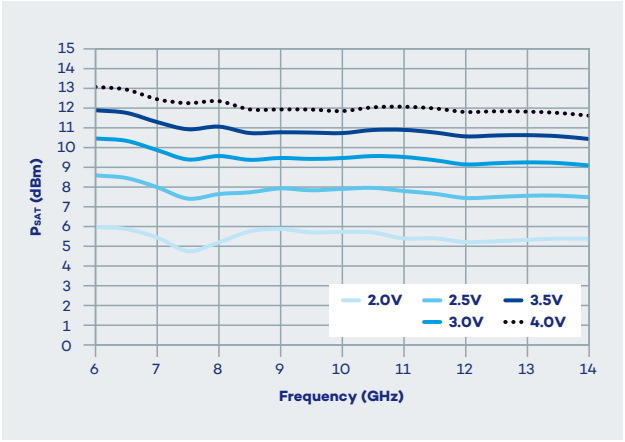
Output Power vs Input Power @V_{DD} = 3V



P1dB vs Frequency vs V_{DD}



P_{SAT} vs Frequency vs V_{DD}



V_{DD} vs I_{DD}

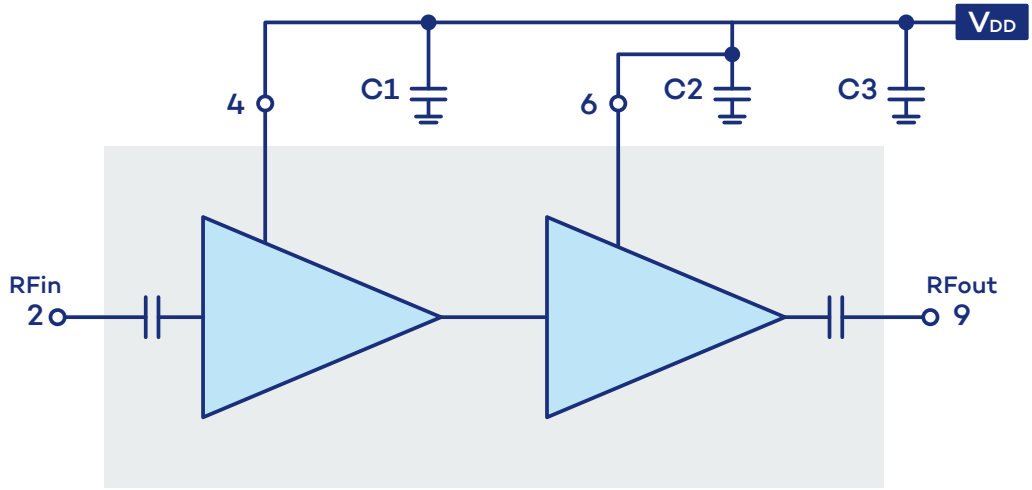
V_{DD}	I_{DD}
2.0V	23mA
2.5V	27mA
3.0V	30mA
3.5V	34mA
4.0V	38mA

Pin description

Pin number	Name	Description	Electrical interface
2	RF in	AC coupled, amplifier input access. Internally matched 50Ω.	
9	RF out	AC coupled amplifier output access. Internally matched 50Ω.	
4, 6	V_{DD1}, V_{DD2}	1st stage and 2nd stage drain biasing access.	
Die bottom	Gnd	Die Bottom must be connected to RF and DC Ground.	

Application circuit

- C1 and C2 = 100pF MIM capacitor (close to the die)
- C3 = 1µF SMD capacitor 0402



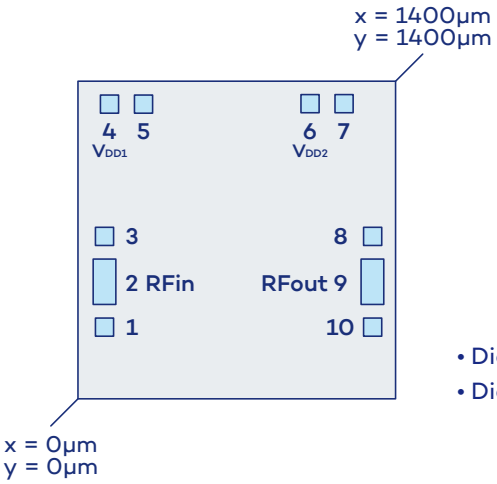
Bias-up procedure

1. Apply V_{DD} = +3V
2. Turn on RF signal

Bias-down procedure

1. Turn off RF signal
2. Reduce V_{DD} to 0V

Die Layout & Pin Out

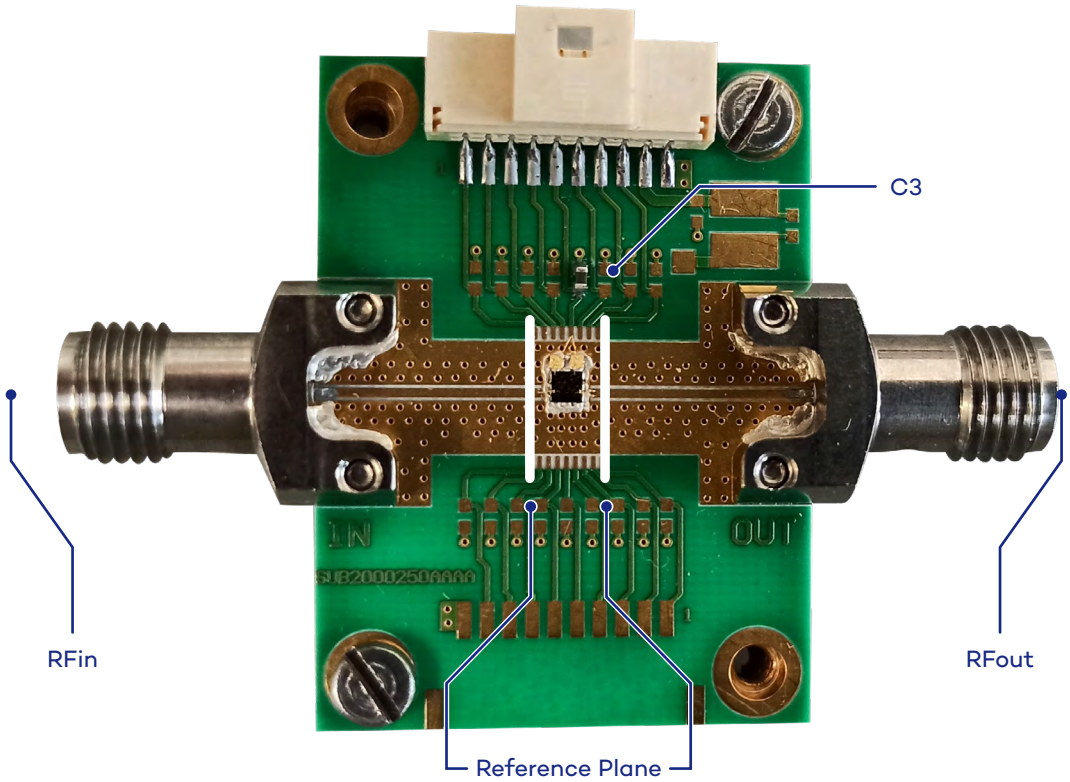


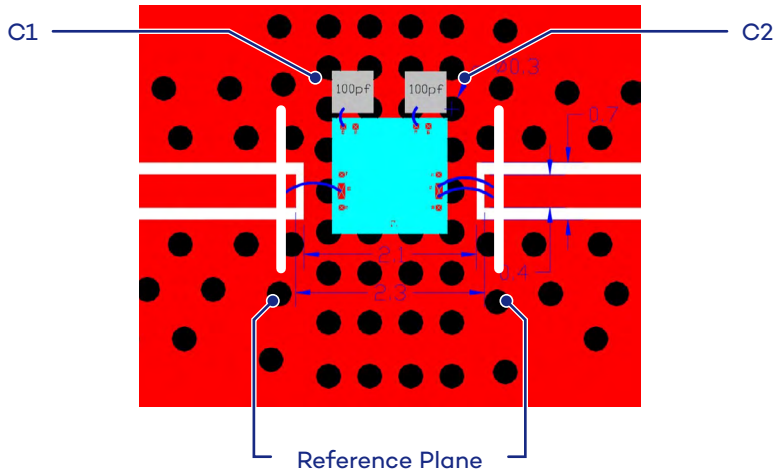
- Die size = 1400µm x 1400µm
- Die thickness = 100µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	117	316	80 x 80	Gnd	
2	117	516	100 x 200	RFin	RF Input
3	117	716	80 x 80	Gnd	
4	139	1299	80 x 80	V_{DD1}	Drain Bias
5	289	1299	80 x 80	Gnd	
6	1023	1301	80 x 80	V_{DD2}	Drain Bias
7	1173	1301	80 x 80	Gnd	
8	1299	716	80 x 80	Gnd	
9	1298	516	100 x 200	RFout	RF Output
10	1299	316	80 x 80	Gnd	

- Die bottom must be connected to ground (RF and DC)

Board Layout





Substrate : RO4350B (εr = 3.48), 0.254mm thickness.

Measurements on connectorized structure. Small signal gain (S21) and Noise figure are de-embedded at reference plane (see drawing above).

Note: Multiple vias should be employed under die to minimize inductance and thermal resistance.

- C1, C2: 100pF MIM capacitor
- RF In: 1 Gold Wire (25µm diameter Au)
- RF Out: 2 Gold Wires (25µm diameter Au each)
- C3: SMD 1µF 0402 capacitor

Ordering information

Product Code	Parameter
VM134D	8 to 12Ghz - 19dB - 1.0dB NF Single bias Low Noise Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

vectrawave.com
+33 (0)2 57 63 00 20
sales@vectrawave.com

Vectrawave Device
5, rue de Louis de Broglie
22300 Lannion
France