

8 to 12GHz - 19dB - 1.0dB NF Single bias Low Noise Amplifier

VM134Q

General Description

The VM134Q is a single bias Low Noise Amplifier designed to operate from 8 to 12GHz.

The device is packaged in a 3x3 mm 16 lead Plastic Surface Mount Package (ROHS). This component uses VM134D Vectrawave MMIC.

The device has a linear gain of 19dB and a typical noise figure of 1.0dB. Typical operating supply current is only 30mA with a supply voltage at +3V. It is manufactured on a PHEMT Technology and is especially suited for radar and for telecommunication applications.

Features

Frequency range	8 – 12GHz
Gain	19dB
Noise figure	1.0dB
Gain flatness	+/-0.5dB
Input return loss	-10dB (Typical)
Output return loss	-12dB (Typical)
Power supply	30mA @ +3V
Package	QFN 3 x 3mm, 16 Lead
Раскаде	QFN 3 X 3mm, 10 Led

Applications

• Radar

- Test and measurement
- Telecommunications

VDD1 VDD2 15 13 16 14 12 1 11 Gnd Gnd 2 RFin 3 10 RFout Gnd 9 Gnd 4 5 7 6 8

Pins Assignement & Functional Block Diagram

Function	Pin number
NC	1/5/6/7/8/12/13/15
Gnd	2/4/9/11
RF in	3
RF out	10
VDD2	14
Vdd1	16

Electrical Specifications

Test conditions: unless otherwise noted

- T_{amb} = +25°C
- IDD = IDD1 + IDD2 = 30mA
- V_{DD} = V_{DD1} = V_{DD2} = +3V

Symbol	Parameter	Min	Тур	Max	Unit
F	Frequency range	8 12			GHz
G	Linear gain	19			dB
ΔG	Small signal gain flatness	+/-0.5			dB
NF	Noise Figure	1.0			dB
OP1dB	Output power @1dB compression	7		dBm	
Psat	Saturated Output Power	9		dBm	
S11	Input return loss	-10		dB	
S22	Output return loss	-12		dB	
VDD1_2	Operating supply voltage	+3		V	
IDD	Supply current	30			mA

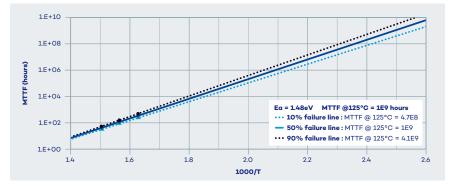
Absolute Maximum Ratings

Symbol	Parameter	Values	Unit
VDD1_2	Drain voltage		V
Pin	CW Input Power	+10	dBm
Tstg	Storage temperature	-55/+125	°C
Тор	Operating temperature	-40/+85	°C
Tch	Channel temperature	+150	°C

Operation of this device above any of these parameters may cause permanent damage.

• MTTF (Provided by Foundry)

0.15µm Low noise pHEMT (PL15-10) vs MTTF Test Arrhenius Plot



The values shown here are calculated, only to be used as a guideline and represent reliability information under Vds = +5V and drain current of 267mA/mm.

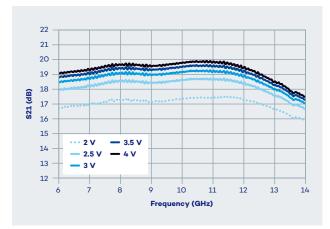


• Typical Performance (Board Measurements)

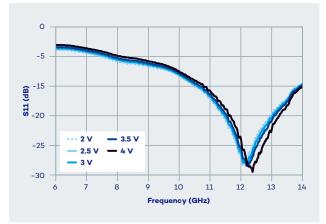
Small Signal Gain vs VDD

Test conditions: unless otherwise noted

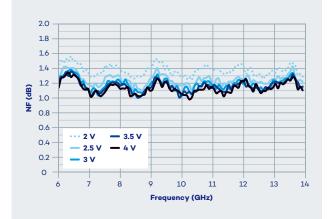
- Reference plane: Component access
- Tamb = +25°C



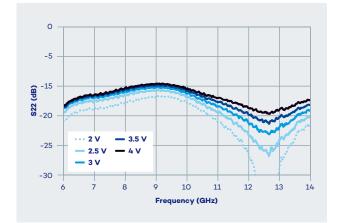
Input Return Loss vs VDD



Noise Figure vs VDD



Output Return Loss vs VDD



• Typical Performance (Board Measurements)

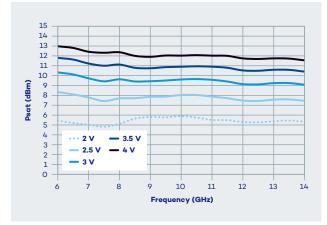
Pout vs Pin vs Frequency

Test conditions: unless otherwise noted

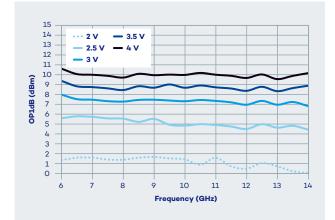
- Reference plane: Component access
- T_{amb} = +25°C
- IDD = 30mA
- V_{DD} = +3V

10 8 6 4 2 Pout (dBm) ···· 7 GHz 0 ••• 8 GHz -2 ••• 9 GHz — 10 GHz -4 — 11 GHz -6 - 12 GHz -8 -10 -25 -23 -21 -19 -17 -15 -13 -11 -9 -7 -5 -3 -1 Pin (dBm)

PSAT VS Frequency VS VDD



P1dB vs Frequency vs VDD



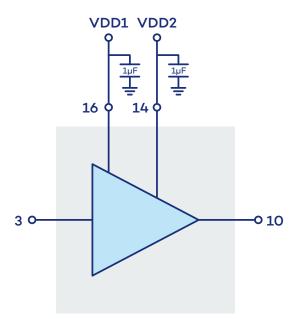
VDD VS IDD

Vdd	Idd
2.0V	23.5mA
2.5V	27.0mA
3.0V	30.0mA
3.5V	34.0mA
4.0V	38.0mA



• Application circuit

1 µF SMD Capacitors as close as possible to the QFN.



• Bias-up procedure

- 1. Apply V_{DD1} = +3V
- 2. Apply V_{DD2} = +3V
- 3. Turn on RF signal

• Bias-down procedure

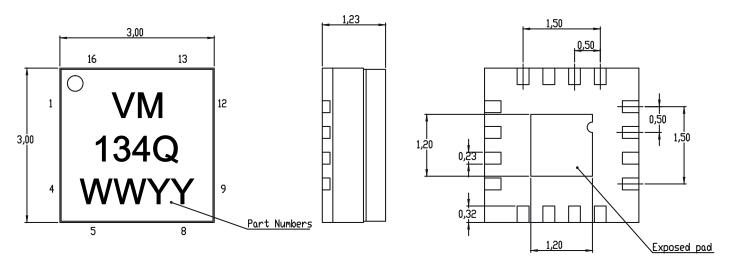
- 1. Turn off RF signal
- 2. Reduce VDD2 to OV
- 3. Reduce V_{DD1} to OV

• Pin description

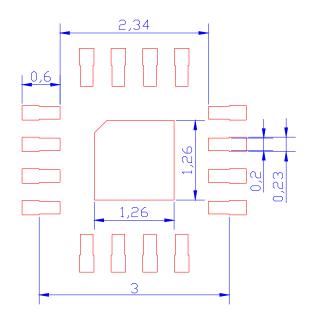
Pin number	Name	Description	Electrical interface
3	RF in	AC coupled, amplifier input access. Internally matched 50Ω .	
10	RF out	AC coupled amplifier output access. Internally matched 50Ω.	RF out
14	VDD2	2 nd stage drain biasing access.	O VDD1_2
16	Vdd1	1 st stage drain biasing access.	•–Ę
Exposed Pad	Gnd	Ground Pad must be connected to RF and DC Ground.	Gnd

Mechanical drawing

1QFN exposed PAD must be connected to ground (RF and DC).

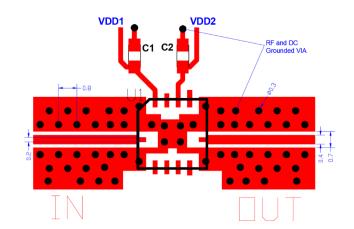


Recommended land pattern



• Suggested Board Layout

C1, C2: 0402 1 µF/16V capacitor Substrate: RO4350B, thickness 0.254mm





Ordering information

Product Code	Parameter
VM134Q	8 to 12GHz - 19dB - 1.0dB NF Single bias Low Noise Amplifier

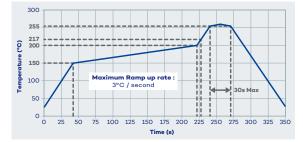
Associated Material

- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability

Solder Stencil thickness: 127µm Solder: SAC 305 (ROHS) Temperature profile example: maximum recommended reflow profile (leadfree)



ESD Sensitivy Rating

Test: Human Body Model (HBM) Std: JEDEC Standard JESD22-A114



Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

RoHS-Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

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