Vectrawave
RF & Millimeter Wave MMIC Design

# 8 to 12GHz - 18dB - 1.0dB NF
Dual bias Low Noise Amplifier

**VM135Q**

## General Description

The VM135Q is a dual bias QFN Low Noise Amplifier designed to operate from 8 to 12GHz. The device is packaged in a 3x3 mm 16 lead Plastic Surface Mount Package (ROHS). This component uses VM135D Vectrawave MMIC.

The device has a linear gain of 18dB and a typical noise figure of 1.0dB. Typical operating supply current is only 28mA with a supply voltage at +3V and -3V. It is manufactured on a PHEMT Technology and is especially suited for radar and for telecommunication applications.

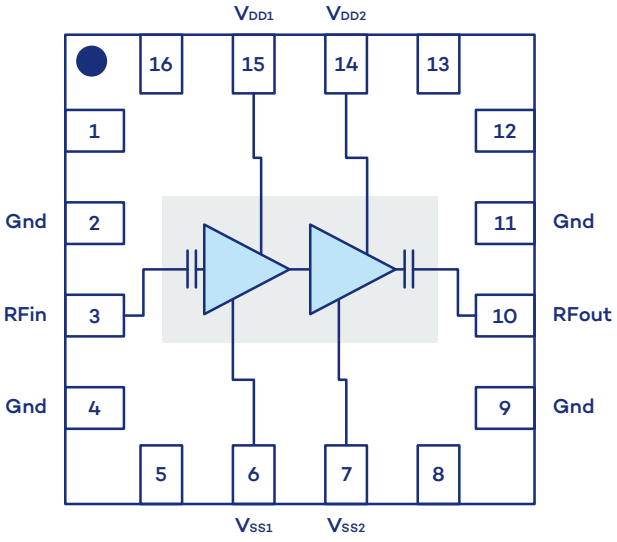
## Features

| | |
|---|---|
| Frequency range | **8 – 12GHz** |
| Gain | **18dB** |
| Noise figure | **1.0dB** |
| Gain flatness | **+/-0.7dB** |
| Input return loss | **-10dB (Typical)** |
| Output return loss | **-12dB (Typical)** |
| Power supply | **28mA @VDD = +3V**<br>**VSS = -3V** |
| Package | **QFN 3 x 3mm, 16 Lead** |

## Applications

- Radar
- Test and measurement
- Telecommunications

## Pins Assignement & Functional Block Diagram




| Function | Pin number |
|---|---|
| NC | 1/5/8/12/13/16 |
| Gnd | 2/4/9/11 |
| RF in | 3 |
| VSS1 | 6 |
| VSS2 | 7 |
| RF out | 10 |
| VDD2 | 14 |
| VDD1 | 15 |

## Electrical Specifications

Test conditions: unless otherwise noted
- Reference plane: component access
- $T_{amb}$ = +25°C
- $V_{DD} = V_{DD1} = V_{DD2}$ = +3V
- $I_{DD} = I_{DD1} + I_{DD2}$ = 28mA
- $V_{SS} = V_{SS1} = V_{SS2}$ = -3V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| F | Frequency range | 8 | | 12 | GHz |
| G | Linear gain | | 18 | | dB |
| ΔG | Small signal gain flatness | | +/-0.7 | | dB |
| NF | Noise Figure | | 1.0 | | dB |
| OP1dB | Output power @1dB compression | | 7 | | dBm |
| Psat | Saturated Output Power | | 9 | | dBm |
| S11 | Input return loss | | -10 | | dB |
| S22 | Output return loss | | -12 | | dB |
| $V_{DD1\_2}$ | Operating supply voltage | | +3 | | V |
| $V_{SS1\_2}$ | | | -3 | | V |
| $I_{DD}$ | Supply current | | 28 | | mA |

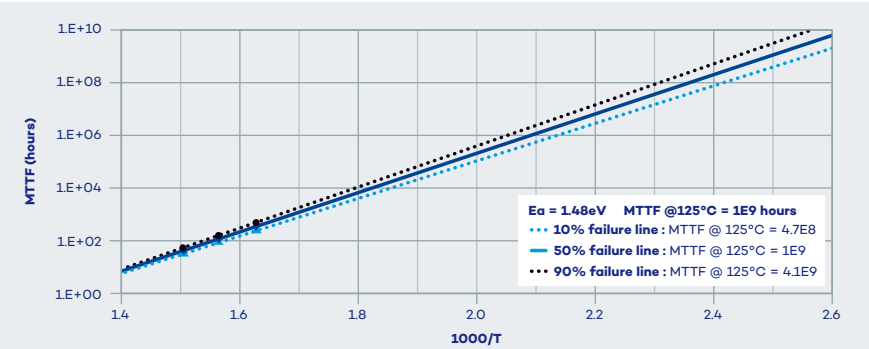
## Absolute Maximum Ratings

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $V_{DD1\_2}$ | Voltage Supply | +4 | V |
| $V_{SS1\_2}$ | | -6/-0.5 | V |
| Pin | CW Input Power | +10 | dBm |
| Tst | Storage temperature | -55/+125 | °C |
| Top | Operating temperature | -40/+85 | °C |
| Tch | Channel temperature | +150 | °C |

Operation of this device above any of these parameters may cause permanent damage.

## MTTF (Provided by Foundry)

### 0.15µm Low noise pHEMT (PL15-10) vs MTTF Test Arrhenius Plot

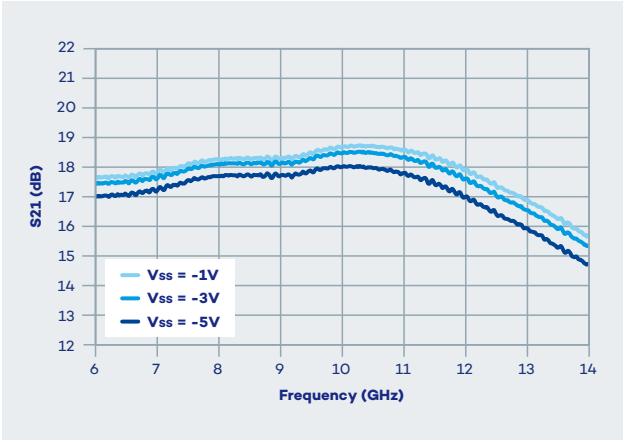



The values shown here are calculated, only to be used as a guideline and represent reliability information under Vds = +5V and drain current of 267mA/mm.

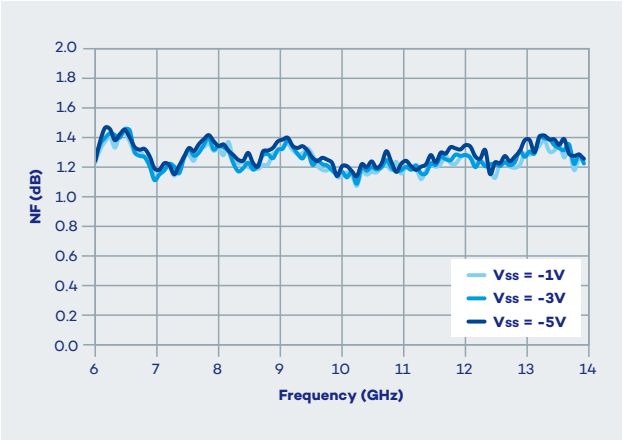
## Typical Performance
### (Small signal / Board Measurement)

Test conditions: unless otherwise noted
Reference plane: component access
- $V_{DD}$ = +3V
- $I_D$ = 28mA (Typically)
- Tamb = +25°C

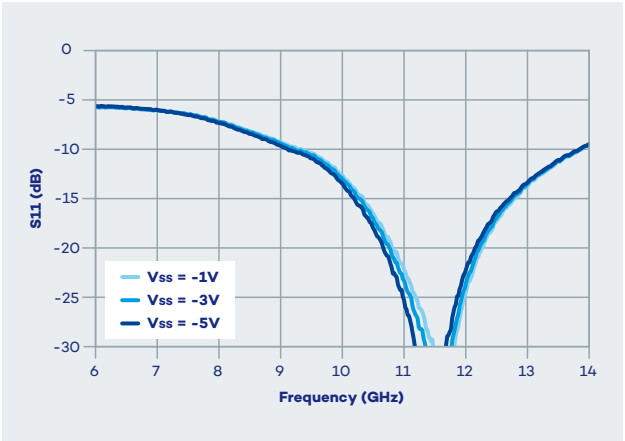
### Small Signal Gain vs Vss



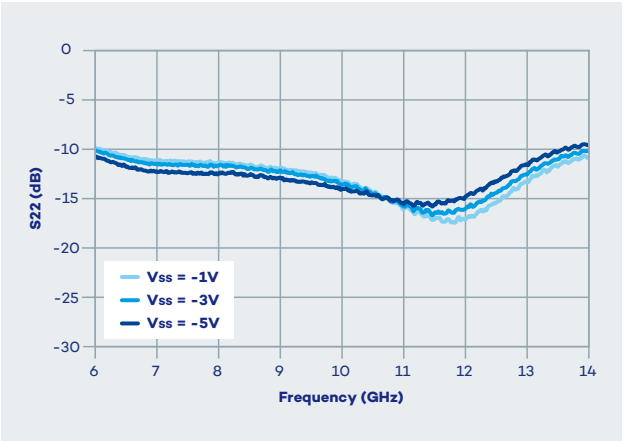

### Noise Figure vs Vss




### Input Return Loss vs Vss



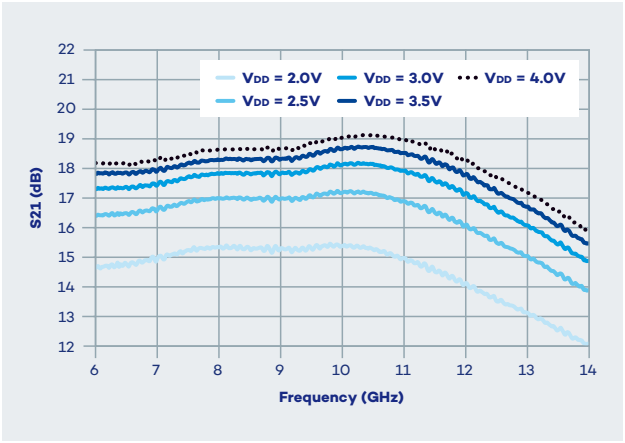

### Output Return Loss vs Vss



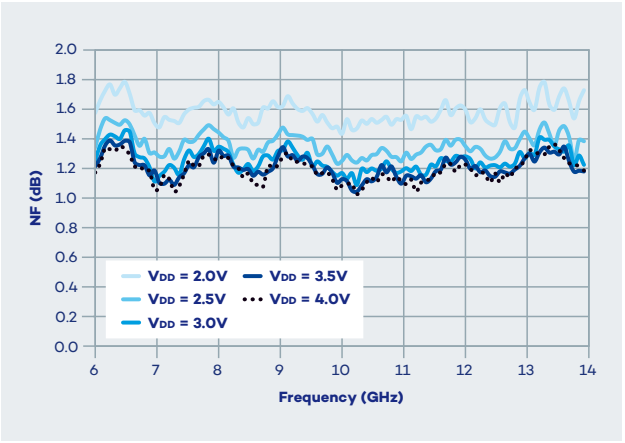
# Typical Performance
## (Small signal / Board Measurement)

Test conditions: unless otherwise noted
Reference plane: component access
- $V_{SS} = V_{SS1} = V_{SS2} = -3V$
- $T_{amb} = +25°C$

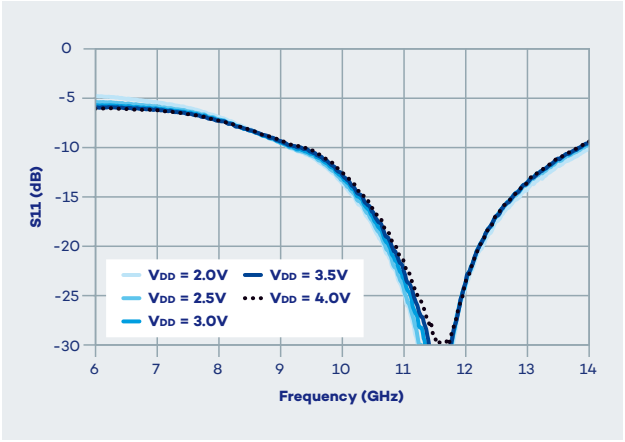
### Small Signal Gain vs $V_{DD}$



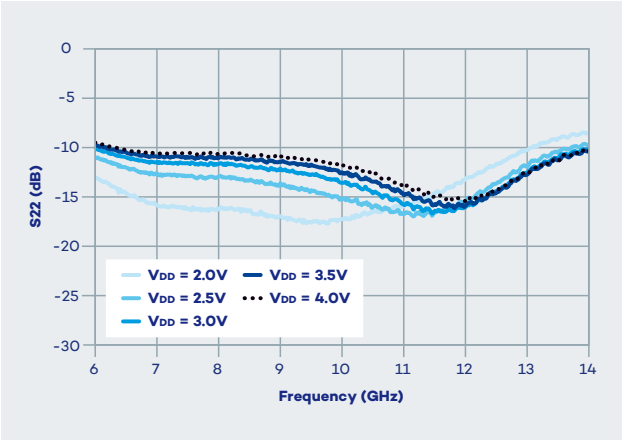

### Noise Figure vs $V_{DD}$




### Input Return Loss vs $V_{DD}$



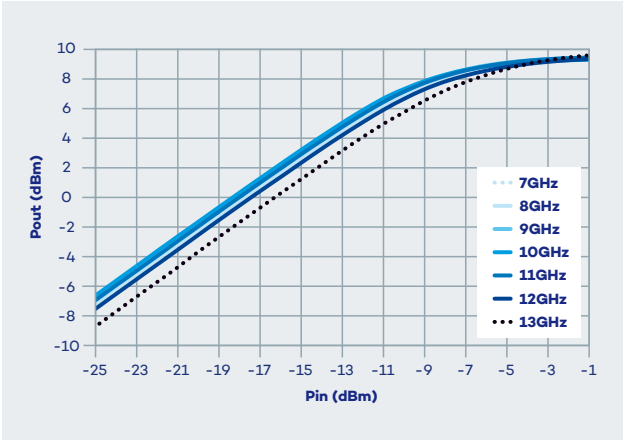

### Output Return Loss vs $V_{DD}$



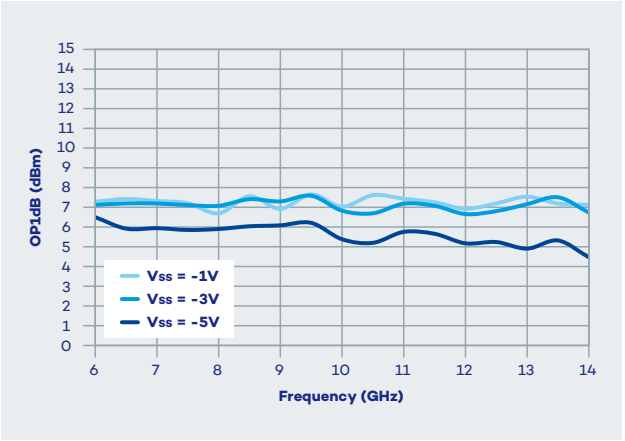
## Typical Performance
### (Large signal / Board Measurement)

Test conditions: unless otherwise noted
Reference plane: component access
- $V_{DD}$ = +3V
- $V_{SS}$ = -3V
- $I_D$ = 28mA (Typically)
- $T_{amb}$ = +25°C

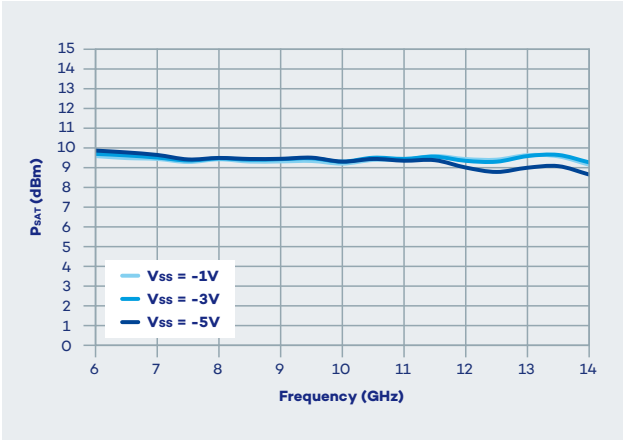
### Pout vs Pin vs Frequency




### P1dB vs Frequency vs Vss




### Psat vs Frequency vs Vss



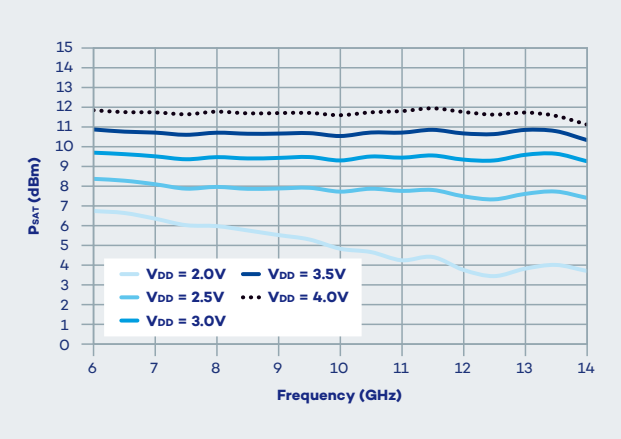

### IDD vs Vss

| $V_{DD}$ (V) | $V_{SS}$ (V) | $I_{DD}$ (mA) |
|---|---|---|
| 3V | -1V | 31mA |
| 3V | -3V | 28mA |
| 3V | -5V | 24mA |

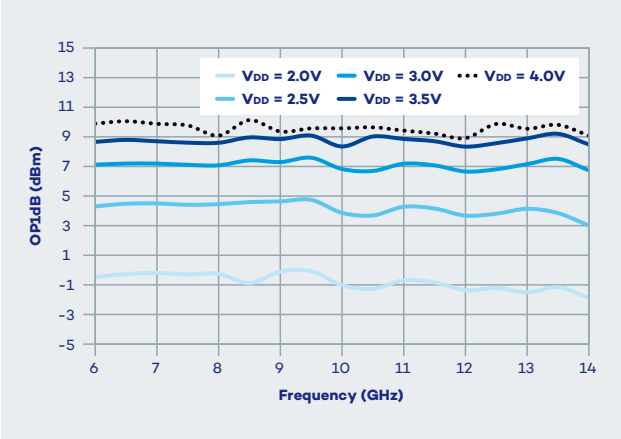
## Typical Performance
### (Large signal / Board Measurement)

Test conditions: unless otherwise noted
Reference plane: component access
- $V_{SS}$ = -3V
- $T_{amb}$ = +25°C

### $P_{SAT}$ vs Frequency vs $V_{DD}$




### P1dB vs Frequency vs $V_{DD}$

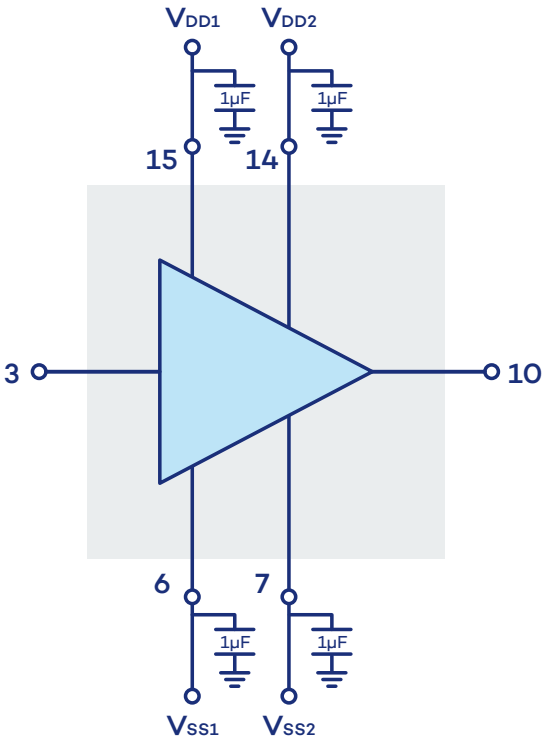



### $I_{DD}$ vs $V_{DD}$

| $V_{DD}$ (V) | $V_{SS}$ (V) | $I_{DD}$ (mA) |
|---|---|---|
| 2V | -3V | 13mA |
| 2.5V | -3V | 20mA |
| 3V | -3V | 28mA |
| 3.5V | -3V | 35mA |
| 4V | -3V | 43mA |

## Application circuit

1 µF SMD Capacitors as close as possible to the QFN.




## Biasing procedure

**Switch on**

1. Apply $V_{SS1}$, $V_{SS2}$ = -3V
2. Apply $V_{DD1}$, $V_{DD2}$ = +3V
3. Turn on RF signal

**Switch off**

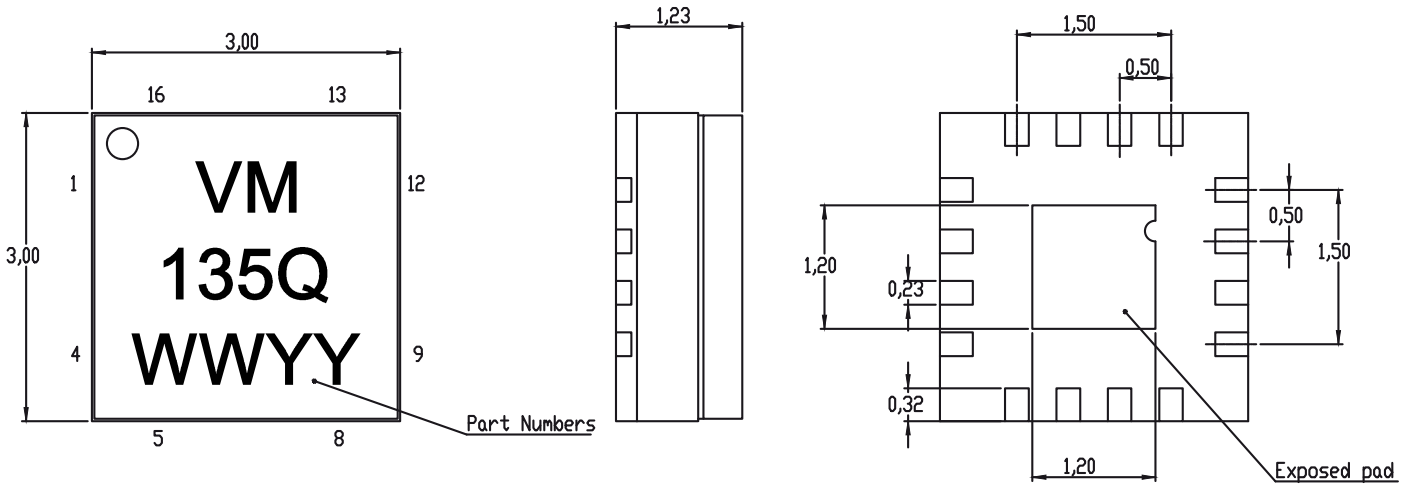
1. Turn off RF signal
2. Reduce $V_{DD1}$, $V_{DD2}$ to 0V
3. Reduce $V_{SS1}$, $V_{SS2}$ to 0V

## Pin description

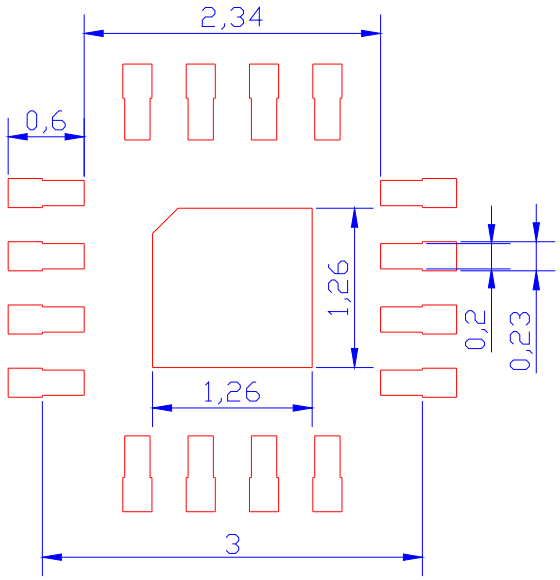
| Pin number | Name | Description | Electrical interface |
|---|---|---|---|
| 2 | RF in | AC coupled, amplifier input access. Internally matched 50Ω. |   |
| 6, 7 | $V_{SS1}$, $V_{SS2}$ | 1st stage and 2nd stage gate biasing access. |   |
| 10 | RF out | AC coupled amplifier output access. Internally matched 50Ω. |   |
| 14, 15 | $V_{DD2}$, $V_{DD1}$ | 2nd stage and 1st stage drain biasing access. |   |
| Exposed Pad | Gnd | Die Bottom must be connected to RF and DC Ground. |   |

## Mechanical drawing

QFN exposed PAD must be connected to ground (RF and DC).

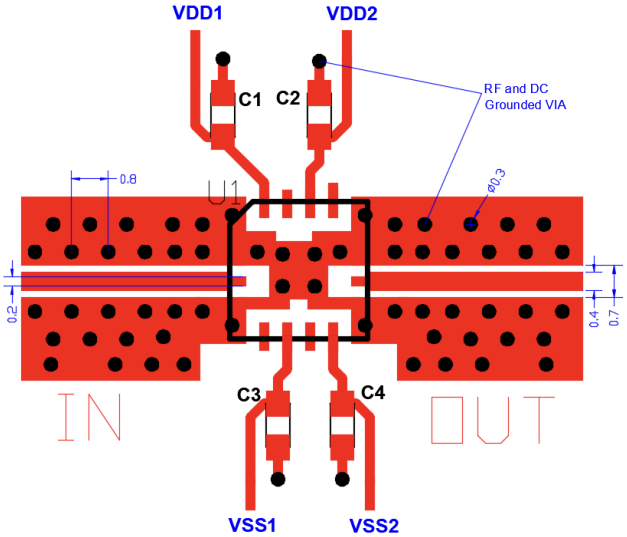



## Recommended land pattern




## Suggested Board Layout

C1, C2, C3, C4: 0402 1 µF/16V capacitor
Substrate: RO4350B, thickness 0.254mm



## Ordering information

| Product Code | Parameter |
|---|---|
| VM135Q | 8 to 12GHz - 18dB - 1.0dB NF Dual bias Low Noise Amplifier |

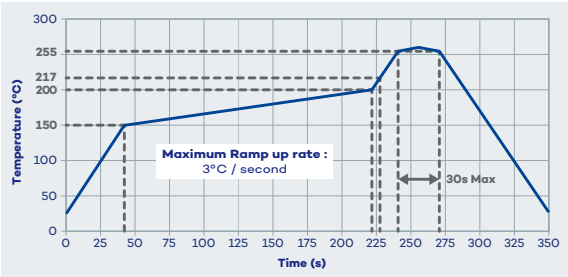
## Associated Material

- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

## Product Compliance Information

**Solderability**

Solder Stencil thickness: 127µm
Solder: SAC 305 (ROHS)
Temperature profile example: maximum recommended reflow profile (leadfree)




**ESD Sensitivy Rating**

Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114


**RoHS-Compliance**

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

**Other attributes**

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

## Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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