

APPLICATION NOTE**Evaluation Board : P/N VWA 0000957 AB****QFN : VWA0000936AD****Distributed Amplifier in QFN 5x5 24L Evaluation Board with DC blocks and Bias-tee**

	Writer	Controller	Approving
Name	CTU	DLB	
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I. HISTORIC

Edition	Date	Description of changes	
1.0	11/12/2017	Creation	

II. REFERENCE DOCUMENTS

Document Title	Reference Document	Date	Edition

III. SUMMARY

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IV.INTRODUCTION

IV-1. Description

The VWA0000957AB is the Distributed Amplifier packaged in QFN and reported on PCB “evaluation board”. It is working in the DC-28 GHz frequency bandwidth. It uses the VWA0000936AD component (VWA50014AA die integrated in 5x5mm plastic QFN).

The evaluation board is composed by 2 mains parts:

- A Distributed Amplifier packaged in QFN (VWA0000936AD) (1)
- A test structure support : PCB with SMA connectors (2)

The QFN VWA0000936AD uses the die VWA50014AA and first order decoupling components in a 5x5mm plastic QFN.

The test structure support uses a RF PCB with SMA connectors, second order decoupling components, 2 DC connectors to bias the component, and a heat sink. It also contains a RFin DC-block, a RFout DC-block and a RFout Bias-tee.

Supply cables are also provided.

This document describes the way to use the evaluation board VWA0000952AB.

RF features and results are not included.

IV-2. Evaluation Board PHOTO

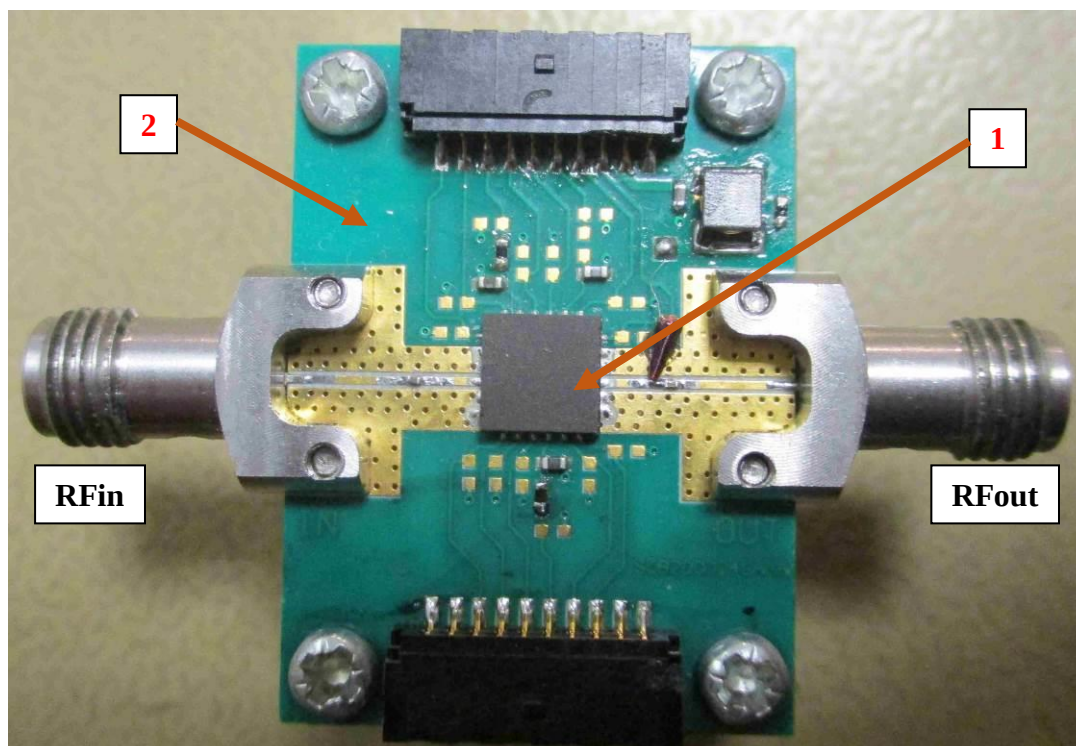


Figure 1: Evaluation board VWA0000957AB photo

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V. INTERFACE AND COMPONENTS

V-1. Evaluation board VWA 0000957 AB Interface

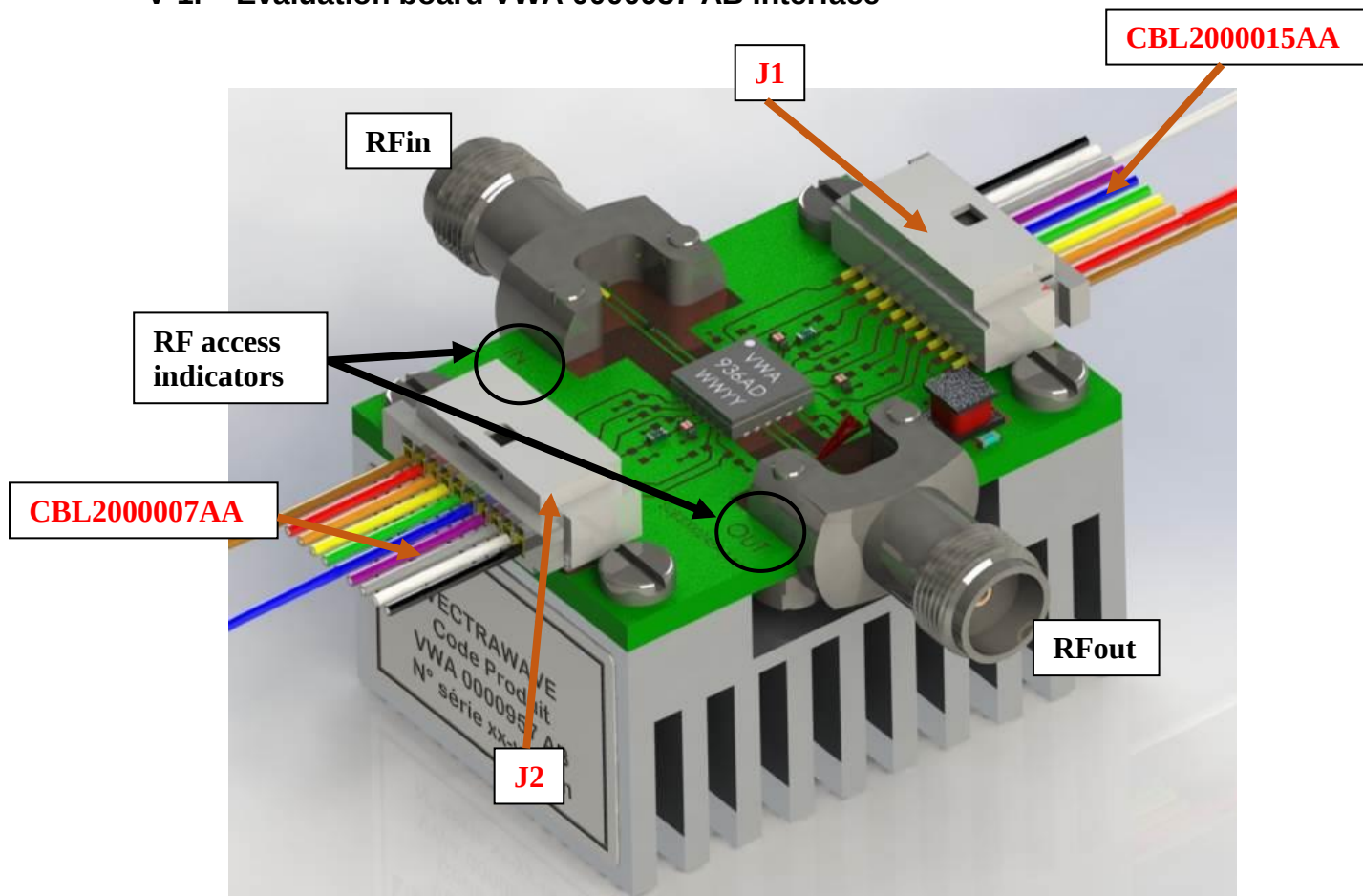


Figure 2: Evaluation board VWA0000957AB interface

Connector	Type	Allocation
J1	SAMTEC T1M-10-F-SH-L	Connect to CBL2000015AA cable : VG2, VBIAS power supply and GND.
J2	SAMTEC T1M-10-F-SH-L	Connect to CBL2000007AA cable : VG1 power supply and GND
RFIN	SMA female	RF Input
RFOUT	SMA female	RF Output

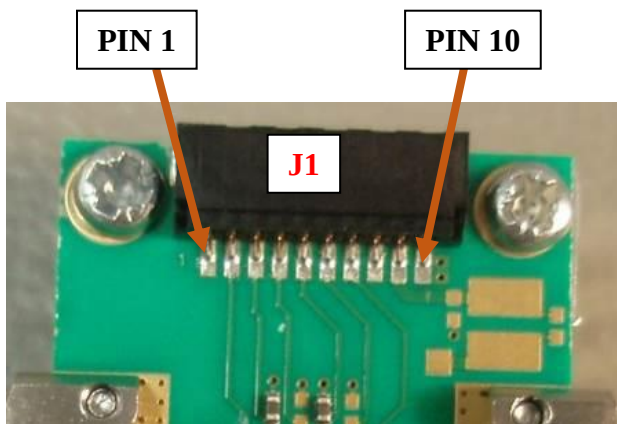


Figure 3: J1 PINOUT

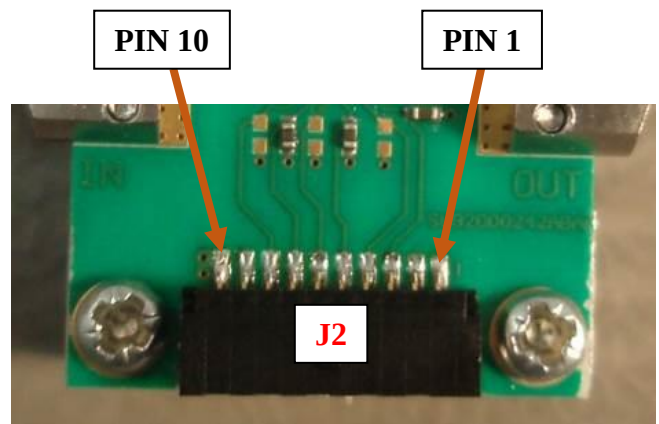


Figure 4: J2 PINOUT

PIN	J1 Identification	J2 Identification
1	NC	NC
2	NC	NC
3	VG2	NC
4	NC	NC
5	NC	VG1
6	NC	NC
7	NC	NC
8	NC	NC
9	VBIAS	NC
10	GND	GND

Figure 5: J1 and J2 PINOUT identification

V-2. PCB layout

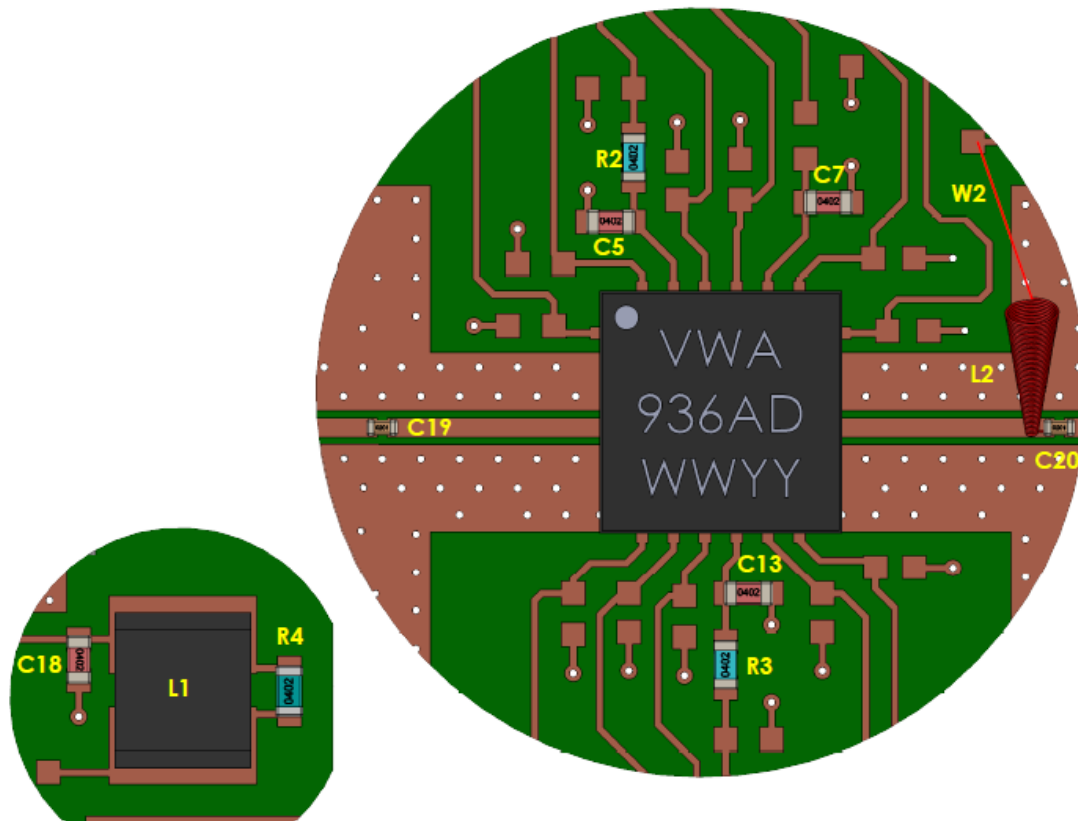


Figure 6: PCB layout

Components	Value	Type
C5,C7, C13, C18	1 μ F/16V	0402
R2, R3	0 Ohms	0402
R4	1KOhms	0402
L1	100 μ H	
L2	1.2 μ H	Conical inductor
C19,C20	220nF	0201

V-3. Interface cable overview

Evaluation board VWA0000957AB interface cable:

- CBL2000015AA on J1 (VG2, VBIAS power supply and GND)
- CBL2000007AA on J2 (VG1 power supply and GND)

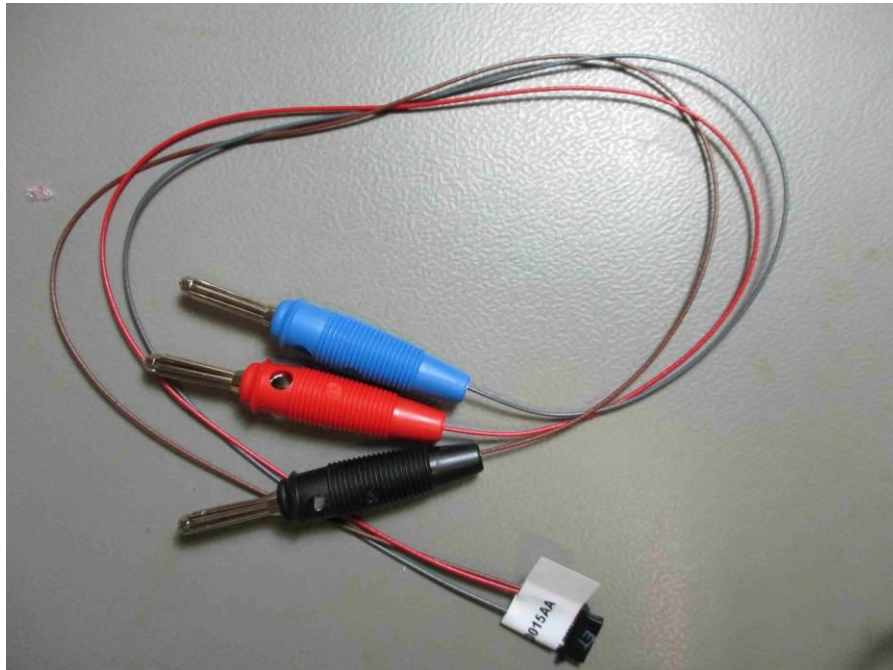


Figure 7: CBL2000015AA

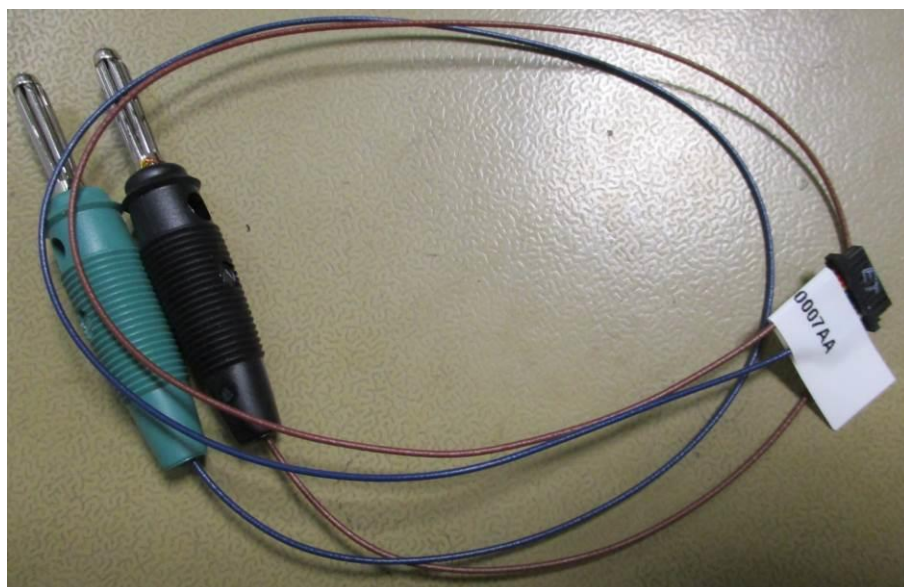


Figure 8: CBL2000007AA

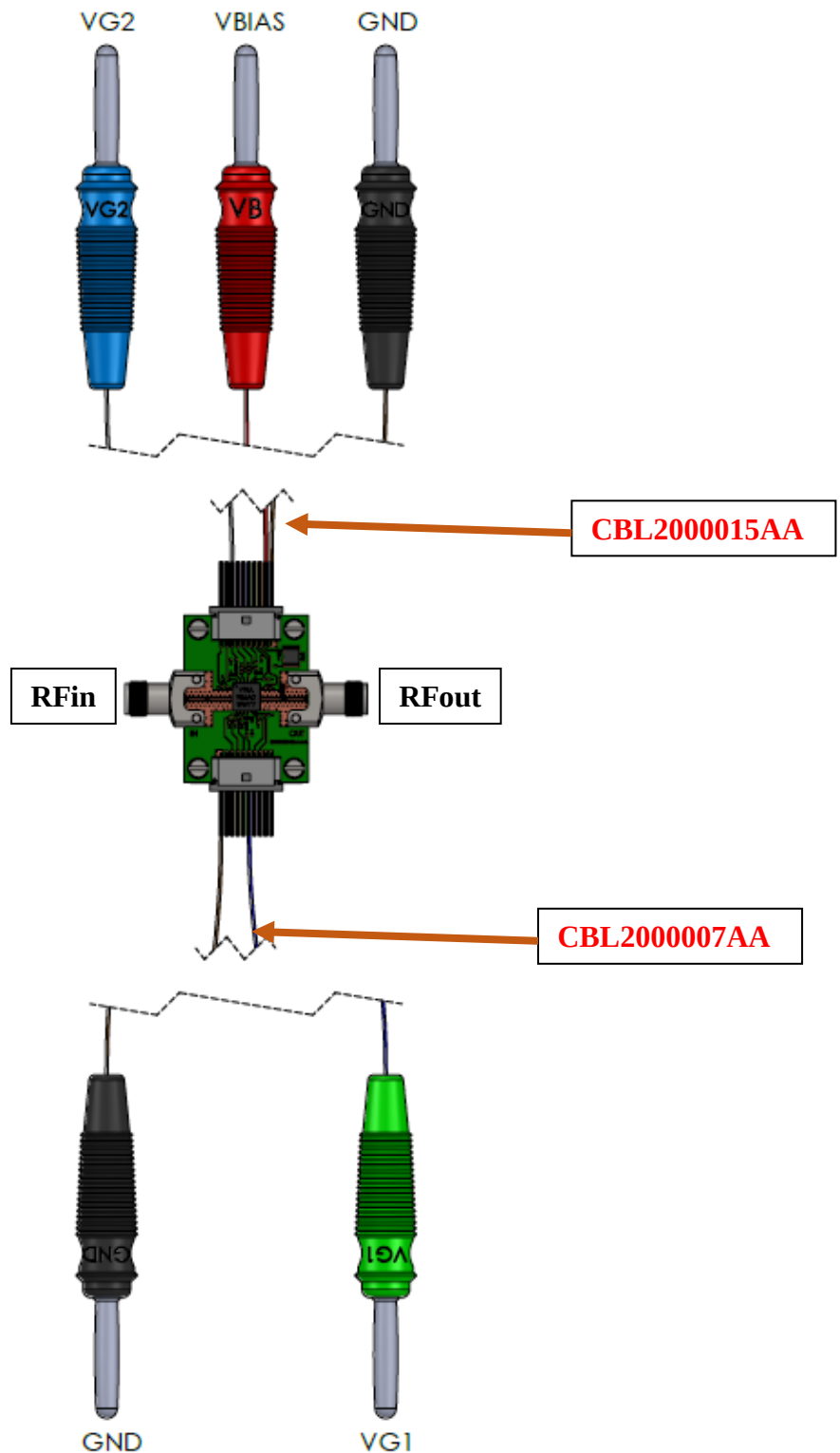


Figure 9: Cable interface

VI. BIASING PROCEDURE AND OPERATING CONDITIONS

Electrical operating conditions

VBIAS = +9.6V

VG2 = 2V

VG1 = 0V

Biasing procedure

Switch on

1. Set VG1 to 0V
2. Set VBIAS to +9.6V
3. Set VG2 to +2V
4. Turn RF ON

VG2 can be tune to adjust linear Gain and Psat.

VG1 can be adjust (from -0.3V to +0.1V) to tune the operating point of the amplification line (Linear application).

Switch off

1. turn RF OFF
2. Set VG2 to 0V
3. Set VBIAS to 0V
4. Set VG1 to 0V

VII. ABSOLUTE MAXIMUM RATINGS

Maximum ratings	Symbols	Min	Max	Units
Drain Voltage	VBIAS		+10	V
Cross point control	VG1	-1.5	+0.15	V
Output amplitude control	VG2	-1	VBIAS/2	V
CW Input Power	Pin		+20	dBm
Junction temperature	Tj		+150	°C
Tstg	Storage Temperature	-55	+125	°C

Operation of this device above any of these parameters may cause permanent damages.

Fin du document