

Test Report

Evaluation Board : P/N VM105QE

VWA0000754AD Evaluation Board

8.5 to 11GHz X-Band Evaluation Board

	Written	Controlled by	Approved by
Name	DLA		
Date	09/09/2025		
Signature	OK		



I. HISTORIC

Edition	Date	Description of Evolutions
1.0	16/02/2025	Creation
1.1	09/09/2025	Modifications (EVB VM105QE)

II. REFERENCE DOCUMENTS

Title of document	Reference of the document	Date	Edition
VWA 500049AA Data Sheet	VWA_500049_AA_DS	03/2015	1.0

III. SUMMARY

I.	Historic.....	2
II.	Summary	2
III.	List of illustration.....	Erreur ! Signet non défini.
IV.	Related documents	2
V.	Introduction.....	3
V-1.	Product Composition / Configuration.....	Erreur ! Signet non défini.
V-2.	Measurement Equipment.....	Erreur ! Signet non défini.
V-3.	Measurement tools.....	Erreur ! Signet non défini.
VI.	Description	Erreur ! Signet non défini.
VII.	tests results	Erreur ! Signet non défini.
VII-1.	Measurements conditions	11
VII-2.	Measurements overview	Erreur ! Signet non défini.
VIII.	Measurements Result Summary	Erreur ! Signet non défini.
IX.	Small signal measurement.....	Erreur ! Signet non défini.
IX-1.	S-parameters	Erreur ! Signet non défini.
IX-2.	Rx Channel Digital attenuator and phase shifter	Erreur ! Signet non défini.
X.	Power measurement	Erreur ! Signet non défini.
X-1.	Rx channel	Erreur ! Signet non défini.
X-2.	Tx channel	Erreur ! Signet non défini.



IV. INTRODUCTION

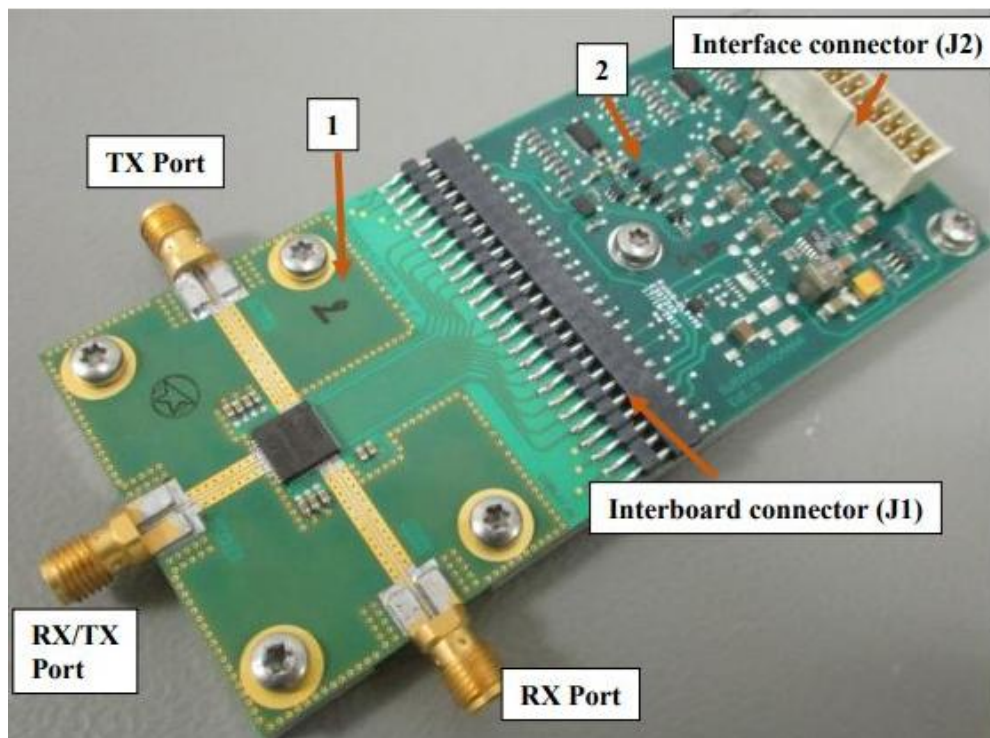
IV-1. Description

VWA000754AD is a multifunction core chip « Evaluation Board » using VWA0000950AA (8.5 to 11GHz) X band core chip in QFN 7x7mm 48 Lead. The Evaluation board is composed with 2 mains parts :

- RF Board VWA1000822 AD (1)
- Interconnection Board VWA1000823 AA (2)
- RF Boards uses the SFN VWA0000950 AA with X band core chip inside (VWA5000049 AA die).
- Interconnection Board VWA 1000823 AA is Analog interface to drive X band core chip. It generates regulated supplies and drives TTL logic signal for RX/TX commutation, the 5bit Attenuator and the 6bits Phase shifter. Timing sequence for biasing procedure is integrated on board.

This document describes the way to use analog interface for the core chip test. RF features and results are not included. (For electrical and RF parameters, see data sheet VWA_500049_AA_DS).

IV-2. Photo of the Evaluation Board



V. INTERFACE BOARD ACCESS

The VWA0000754AD is easy to set up to evaluate the performance of VWA0000950AA X band core chip in QFN 7x7mm 48 Lead with its interface board.

The main accesses are available via Interface connector (J2) to control core chip.

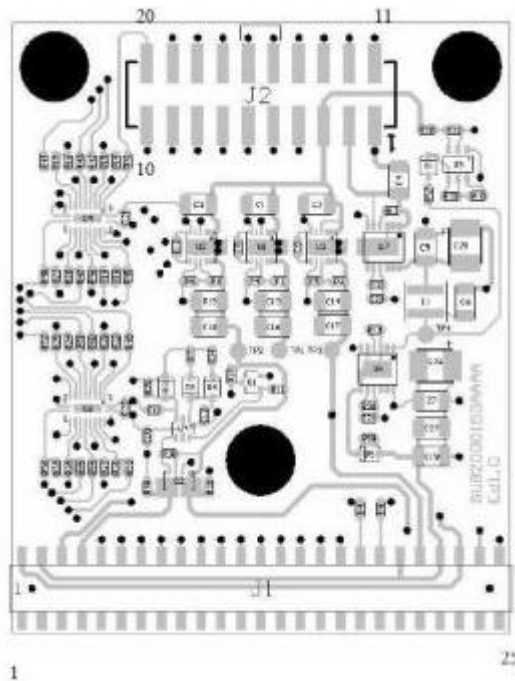
V-1. Interface : INPUT connector Pinout

J2 Connector → reference: IPL1-110-02-L-D-K (SAMTEC)

Pin number	Label	Description
1	Ground	
2	-6V	Negative supply
3	+6V	Positive supply
4	Not used	
5	Not used	
6	Not used	
7	Not used	
8	Not used	
9	Rx S	TTL control TX/RX mode commutation
10	A4	TTL control Attenuator Bit 5
11	A3	TTL control Attenuator Bit 4
12	A2	TTL control Attenuator Bit 3
13	A1	TTL control Attenuator Bit 2
14	A0	TTL control Attenuator Bit 1
15	P5	TTL control Phase shift Bit 6
16	P4	TTL control Phase shift Bit 5
17	P3	TTL control Phase shift Bit 4
18	P2	TTL control Phase shift Bit 3
19	P1	TTL control Phase shift Bit 2
20	P0	TTL control Phase shift Bit 1

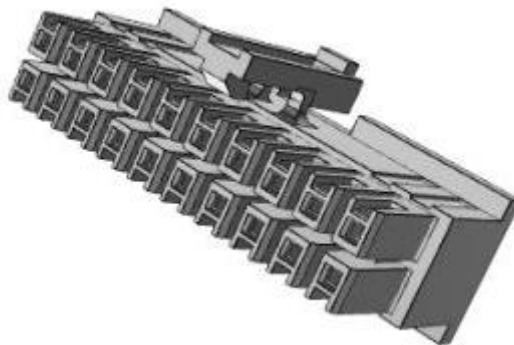


V-2. Interface Board View



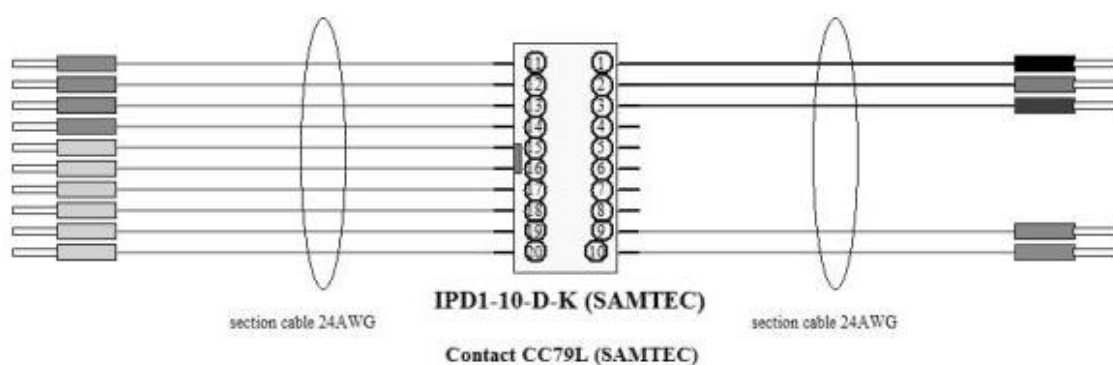
V-3. Interface cable overview

J2 is a 20 pins connector IPL1-110-02-L-D-K from SAMTEC, it makes with IPD1-10-D-K from SAMTEC with Contact CC79L.



PD1-10-D-K from SAMTEC





Cable realization example

V-4. Features and recommended operating conditions

Operating conditions : J2 Input DC-DC Voltage

Parameter	Pin number	Unit	Min.	Typ.	Max.
Positive supply (1)	3	V	5	+6	+8
Negative supply (2)	2	V	-8	-6	-5.5
TTL input Low Level (3)	9 to 20	V	-	0	0.4
TTL input High Level (3)	9 to 20	V	3	5	7

(1) Positive supply is regulated in the board to generate each supply positive voltage for chip core (+4V and +3.3V)

(2) Negative supply is regulated in the board to generate each supply negative voltage for chip core (-5V)

(3) the TTL inputs are tied to the ground with 10K Ω resistor.

VI. QUICK START PROCEDURE

1. Apply Negative Voltage (Pin 2/J2) : Typ. -6V, consumption must be <30mA.
2. Apply Positive Voltage (Pin 3/J2) : Typ. +6V, consumption must be <400mA (in all configuratuib)
3. Select Tx or Rx operating mode (Pin9/J2). This pin tied ground (0V) set the chip Core in Rx mode. Apply High TTL level voltage (+5V) in Tx mode.
4. Use TTL control bits for Attenuators adjustment (Pin 10 to 14/J2) :

Attenuator value	EA0	EA1	EA2	EA3	EA4
0dB	0	0	0	0	0
0.9dB	1	0	0	0	0
1.8dB	0	1	0	0	0
3.6dB	0	0	1	0	0
7.2dB	0	0	0	1	0
14.4dB	0	0	0	0	1

Low level 0 → 0V ; High level 1 → +5V

5. Use TTL Control bits for Phase adjustment (Pin 15 to 20/J2) :

Attenuator value	EP0	EP1	EP2	EP3	EP4	EP5
0°	0	0	0	0	0	0
5.625°	1	0	0	0	0	0
11.25°	0	1	0	0	0	0
22.5°	0	0	1	0	0	0
45°	0	0	0	1	0	0
90°	0	0	0	0	1	0
180°	0	0	0	0	0	1

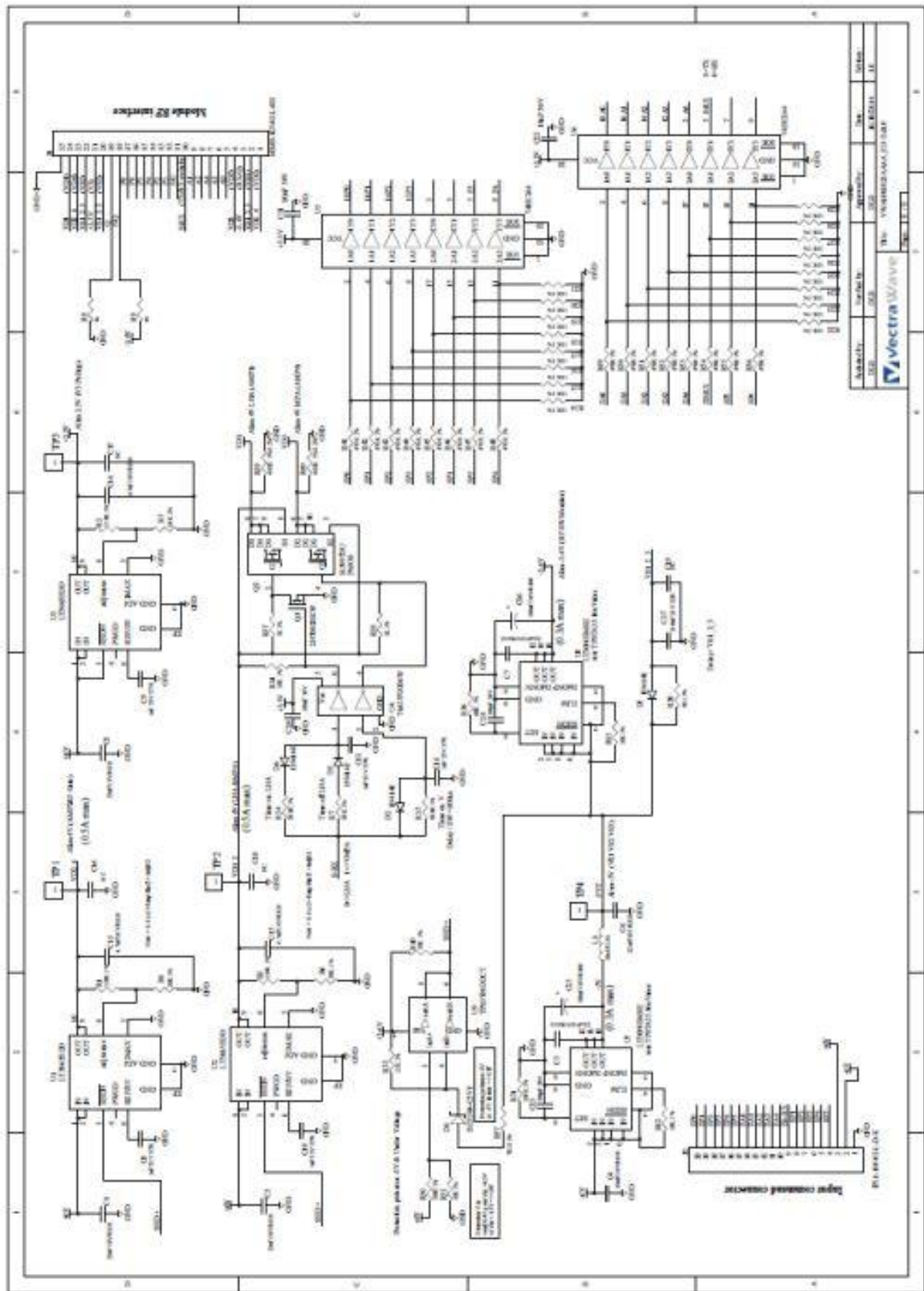
Low level 0 → 0V ; High level 1 → +5V



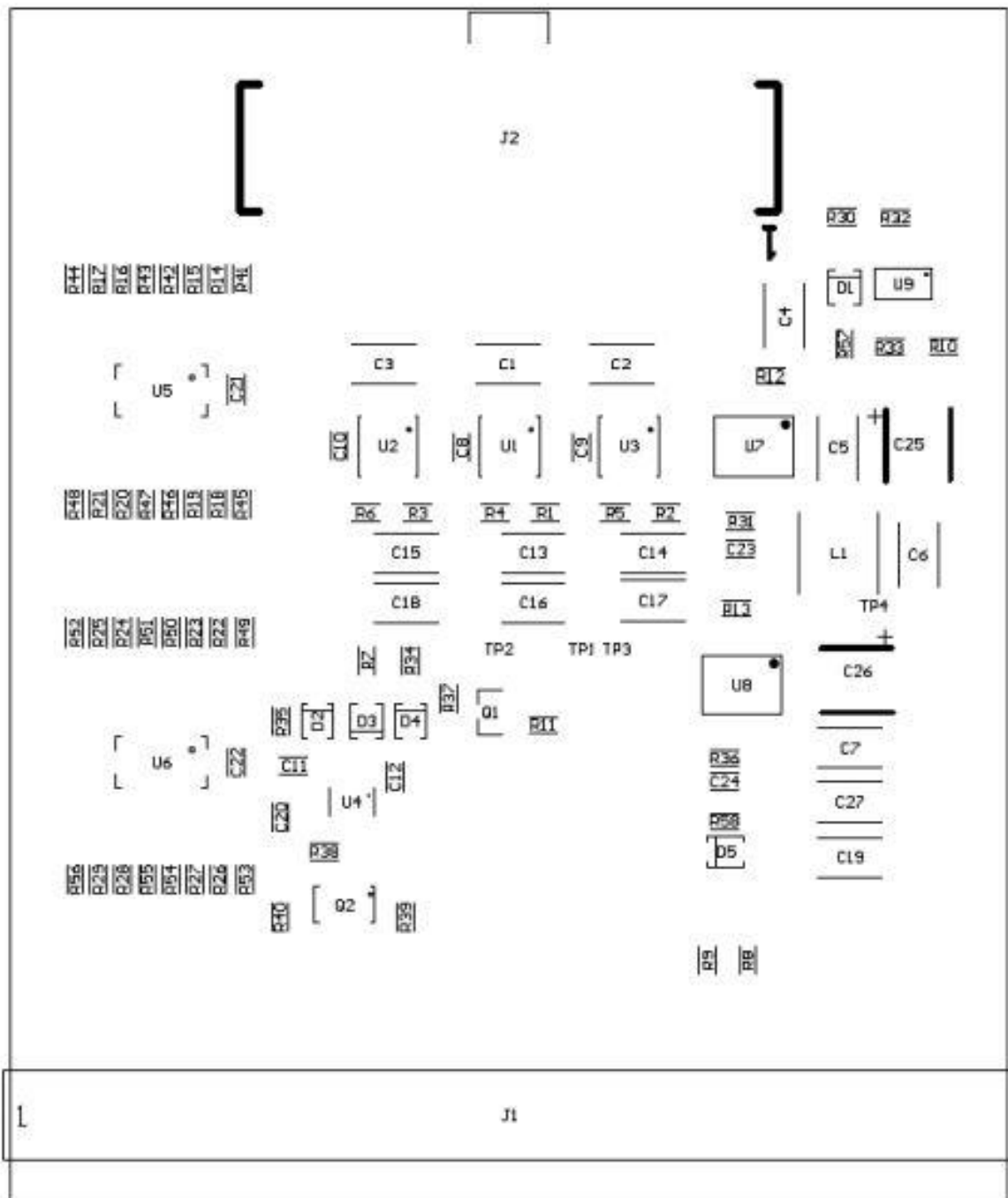
6. The Interface board Design takes into account security device and sequencing voltage during switching Rx/Tx mode.

- If negative supply voltage is not applied, positive voltage doesn't occur.
- If positive voltage under 4.5V, the device is OFF (no positive voltage applied on Chip Core).
- In Rx mode : MPA is switched OFF and LNA is ON.
- In Tx mode : LNA is switched OFF and MPA is ON.

VII. ANNEX 1 (VWA1000823 AA SCHEME)



VIII. ANNEX 2 (VWA1000823 AA PCB OVERLAY)



IX. ANNEX 3 (VWA1000823 AA OUTPUT CONNECTOR J1 PIN OUT)

J1 Connector → reference: MMS-125-02-L-SH (SAMTEC)

Pin number	Label	Description
1	VD2	+4V Common Amplifier supply
2	VS1	-5V Gate Bias
3	RX-Q	RF switch monitor
4	VD3	+4V MPA supply
5	A0	TTL control Attenuator Bit 1
6	A3	TTL control Attenuator Bit 4
7	A4	TTL control Attenuator Bit 5
8	A2	TTL control Attenuator Bit 3
9	A1	TTL control Attenuator Bit 2
10	S-RX	TTL control TX/RX switch
11	Not Used	
12	P5	TTL control Phase shift Bit 6
13	P2	TTL control Phase shift Bit 3
14	P4	TTL control Phase shift Bit 5
15	P3	TTL control Phase shift Bit 4
16	P1	TTL control Phase shift Bit 2
17	P0	TTL control Phase shift Bit 1
18	NQ	No connected
19	Q	No connected
20	VS2	-5V Gate Bias
21	+3.3V Pull up	On chip pull-up (Logic control)
22	VS3	-5V Gate Bias
23	VD4	+4V Gate Bias (>0)
24	VD1	+4V LNA Supply
25	GND	Ground

End of document

